

Two Novel Phase-Frequency Detectors

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Abstract— This paper describes two novel phase-frequency detectors. The first one overcomes the non-linear transfer characteristic found in many conventional phase-frequency detectors and thus results in a PLL-VCO with low phase noise. The second phase-frequency detector can be used in a Phase Locked Loop (PLL) to recover the carrier of a Binary Phase Shift Keyed (BPSK) signal, thus permitting the BPSK data to be demodulated with hardware that is significantly simpler and performs better than the Costas Loop [1].

Keywords—Phase Detector, PLL, XOR Phase detector, Phase Frequency Detector, BPSK Phase Detector, Costas Loop.

I. INTRODUCTION

There are two types of phase detectors in common use. The first type produces a narrow pulse during the time difference between the falling edge of the Reference signal (R) and Voltage Controlled Oscillator (VCO) output signal (V) as shown in Fig. 1.

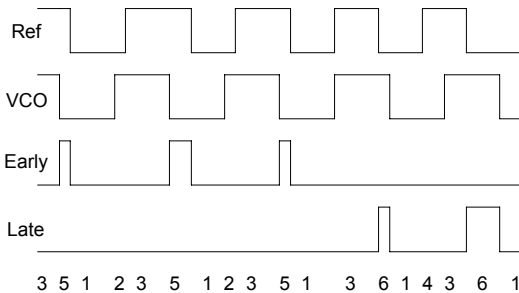


Figure 1. Pulsed phase-frequency detector waveforms.

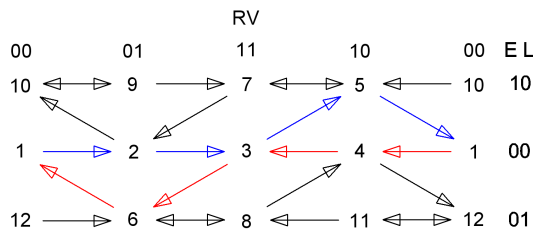


Figure 2. Pulsed phase-frequency detector logic signal flow graph.

The logic signal flow graph, developed by the author [2], is a good way of representing the transitions between states for asynchronous sequential logic circuits like phase detectors. It is a simple graphical diagram to represent all the possible transitions for the asynchronous sequential circuit.

The columns represent the input conditions and sufficient rows are used to ensure that all possible stable states can be accommodated. A different row is used for each output state and multiple rows are used if several different states have the same input and output. To keep the diagram as uncluttered as possible, the states in the left hand column are duplicated in the right hand column. For each input and output, the stable states are shown on the diagram. Arrows between the stable states, show all the possible transitions. Each state should have only one arrow going out to the left and one to the right, but it is possible to have several arrows going to a state. Fig. 2 shows the logic signal flow graph corresponding to Fig. 1. The CD4046 Phase Detector IC, produces waveforms like Fig. 1 and conforms to the logic signal flow graph of Fig. 2. By comparing Fig. 2 of the datasheets for the CD4046 [3] with Fig. 2 in this paper, the advantage of the logic signal flow graph can clearly be seen.

The red and blue lines in Fig. 2, correspond to the transitions between states shown in Fig. 1. The black lines correspond to frequency detection operation.

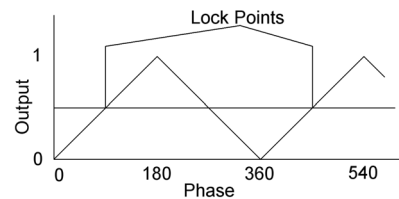


Figure 3. Output voltage versus phase difference for an XOR gate.

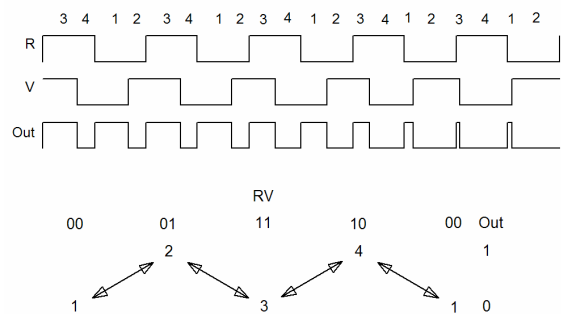


Figure 4. XOR phase detector waveforms and logic signal flow graph.

The second commonly used phase detector is based on a multiplier or Exclusive OR gate. A multiplier produces a sine wave output voltage versus phase difference, while the exclusive OR gate has a triangular output versus phase

difference, as shown in Fig. 3. When the PLL is locked a 90° phase difference exists between the Ref (R) and VCO (V) inputs. When a BPSK modulated signal is applied to the Ref input and the data changes, a 180° phase change occurs, resulting in a 270° phase error, causing positive feedback, and requiring the PLL to slip half a cycle to regain lock. Fig. 4 shows the waveforms and logic signal flow graph for an XOR phase detector.

II. LOW NOISE PHASE-FREQUENCY DETECTOR

The dual output phase detectors of Fig. 1 produce a nonlinearity, similar to crossover distortion in class AB amplifiers, when the phase error changes from an *Early* pulse to a *Late* pulse. The negative feedback of the PLL forces the circuit to operate in this region, resulting in a larger phase noise than is obtained from phase detectors with a single output, like the XOR gate. For this reason, an XOR phase detector is often included as a second phase detector in phase detector IC's like the CD4046. However the XOR phase detector does not have any frequency detection properties and this makes it difficult to obtain reliable frequency locking of the PLL under all operating conditions.

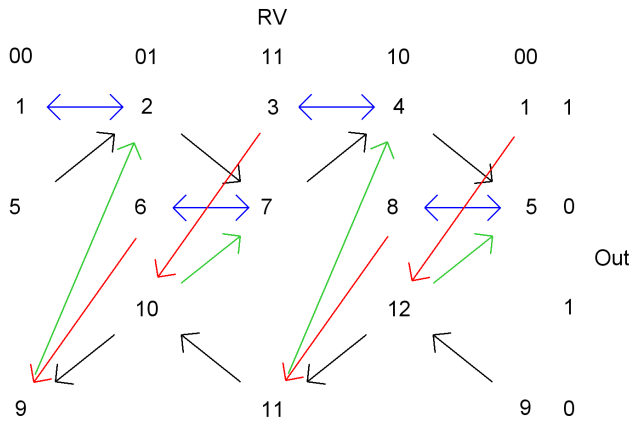


Figure 5. Logic signal flow graph of XOR type phase-frequency detector.

Fig. 5 shows the logic signal flow graph of a new XOR type phase detector, developed by the author, which includes frequency detection properties.

An RV sequence of 00, 01, 11, 10, 00, corresponds to the logic signal flow graph sequence of states: 1, 2, 3, 4, 1 in Fig. 5 and a sequence of states: 5, 2, 7, 4, 5. Both result in the same output waveform. This input sequence corresponds to the stable locking points in Fig. 3. For convenience this RV sequence is called the forward sequence.

When the phase of input V is changed by 180°, a reverse input sequence of RV = 00, 10, 11, 01, 00 results, causing a state sequence of 1, 4, 3, 2, 1 in Fig. 4 and a state sequence 9, 12, 11, 10, 9 in Fig. 5. This corresponds to the unstable 180° to 270° phase region in Fig. 3. When R and V are the same frequency, the logic signal flow graphs of Fig. 4 and 5 give identical outputs regardless of phase difference between R and V, so that these phase detectors behave identical.

In Fig. 5, when V is of a higher frequency than R, an input sequence of RV = 00, 01, 00, 01 causes transitions between states 1 and 2 and an input sequence RV = 11, 10, 11, 10, 11 causes transitions between states 3 and 4. Both result in an output of 1. When R is of a higher frequency than V, transitions between states 6 and 7 or between 5 and 8 occur, which cause a 0 output. The blue transitions in figure 5 correspond these transitions and demonstrate the frequency detection properties of the phase-frequency detector. Finally the red and green state transitions in Fig. 5 ensure that transitions between the forward and reverse sequence occur in a correct manner.

The PLL is considered to be locked during the forward sequence, so that states 5, 2, 7, 4 can be used to produce a phase lock (Lock) output. All other states will only occur when the PLL is unlocked.

The hardware required to implement this phase detector can be designed using asynchronous sequential logic design techniques [2]. The actual design is beyond the scope of this paper. The resulting realization requires three feedback variables F, G and H as shown in Fig. 6.

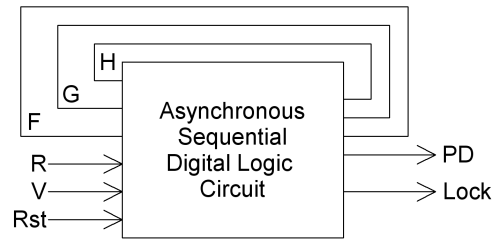


Figure 6. Hardware realisation of the phase-frequency detector.

The inputs to the circuit are the phase detector inputs R and V and a reset Rst. The reset allows the circuit to be initialized to a specific state for functional simulation as part of the VHDL implementation. The outputs from the circuit are the phase detector output (PD) and the phase lock output (Lock). The resulting ABEL equations for the circuit are:

$$\begin{aligned}
 F &= (!R\&H\&F \# R\&!H\&F \# V\&G\&F \# !V\&!G\&F \# V\&!R\&H\&G \\
 &\# V\&R\&!H\&G \# !V\&!R\&H\&G \# !V\&R\&!H\&G) \& Rst \\
 G &= (V\&R\&H\&G\&F \# !V\&!R\&H\&G\&F \# V\&R\&!H\&G\&F \# \\
 &!V\&!R\&!H\&G\&F \# V\&!R\&!H\&G\&F \# V\&R\&H\&!G\&F) \& Rst \\
 H &= (!V\&R\&!H\&G\&F \# V\&!R\&!H\&G\&F \# !V\&R\&H\&!G\&F \# \\
 &V\&!R\&H\&!G\&F \# !V\&!R\&H\&G\&F \# V\&R\&!H\&!G\&F) \& Rst \\
 PD &= !V\&!R\&H \# V\&R\&!H \# V\&R\&F \# !V\&!R\&F \# \\
 &!V\&!H\&G\&F \# V\&H\&!G\&F \\
 Lock &= !V\&R\&H\&F \# V\&!R\&!H\&F \# !V\&!R\&G\&F \# \\
 &V\&R\&!G\&F
 \end{aligned}$$

The design verification must test all transitions in order to ensure that no glitches occur in the simulation. These equations were implemented in VHDL and programmed into a Lattice M4A5 CPLD. The circuit performed as expected, as shown in Fig. 7. The left waveforms, where Lock = 1, correspond exactly to those of Fig. 4. The Lock output is high when the input is a forward sequence. The frequency detection operation is shown in Fig. 8. The PD output is low

on average when the VCO frequency (V) is too high and is high on average when the VCO frequency is too low, thus changing the VCO frequency to ensure the PLL always locks to the reference signal (R). The PLL will always lock with V leading R by 90° .

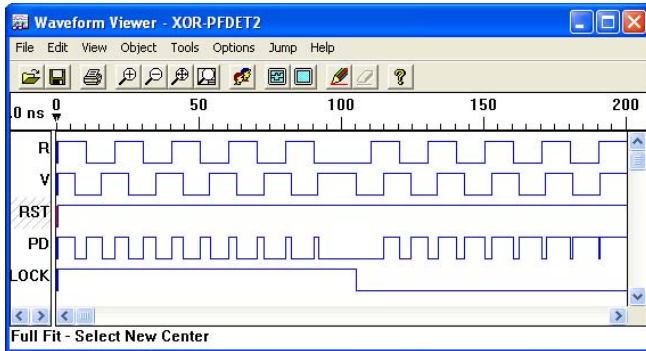


Figure 7. Hardware waveforms for the phase-frequency detector.

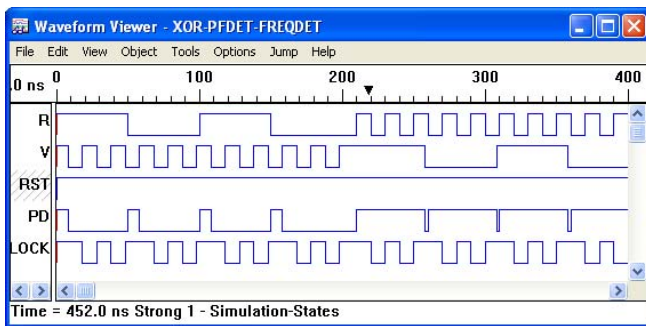


Figure 8. Frequency detection operation of the phase-frequency detector.

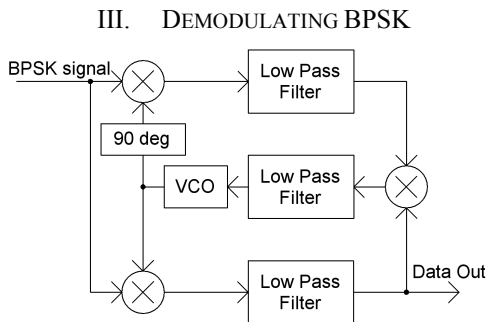


Figure 9. Block diagram for BPSK demodulation using a Costas Loop.

Many communication systems use a BPSK modulated carrier for an RF signal. The conventional method of recovering the carrier of a BPSK signal is to use a Costas Loop [1], the block diagram of which is given in Fig. 9. If a phase detector can be made to detect the phase of a BPSK carrier, then a conventional PLL design can be used to lock onto the carrier and hence demodulate the BPSK signals as shown in Fig. 10. At lower frequencies, it is possible to recover the BPSK data using digital techniques [4, 5] however a PLL can lock onto and remain locked onto the BPSK carrier under lower Signal to Noise Ratio (SNR) conditions or when the input signals are a high frequency.

By comparing Figs. 9 and 10, it can be seen that the block diagram for using a PLL to demodulate BPSK signals is much simpler. Conventional phase detectors cannot lock onto BPSK signals, so that special phase detectors need to be developed to permit the system shown in Fig. 9 to be realized. To provide the lowest phase noise, and XOR type phase detector is desirable.

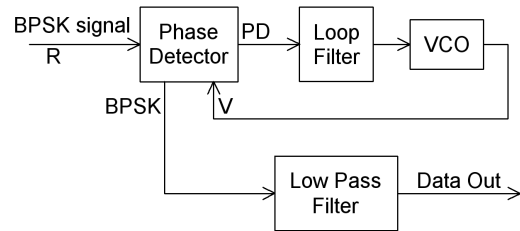


Figure 10. Block diagram for BPSK demodulation using a PLL.

IV. BPSK PHASE DETECTOR DESIGN

For a phase detector, which can satisfy the requirements for Fig.10, the PLL must remain locked when a 180° phase change occurs. A phase detector transfer function shown in Fig. 11 satisfies this. A 180° phase change of the BPSK signal will shift the PLL operating point from the stable lock point of 90° to the stable lock point of 270° , so that the PLL will remain locked, allowing the BPSK data to be demodulated correctly.

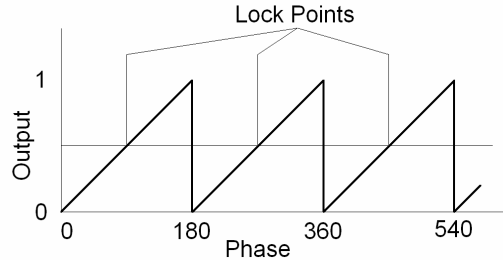


Figure 11. Output versus Phase Difference for the BPSK Phase Detector.

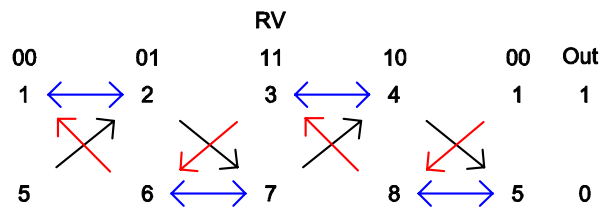


Figure 12. BPSK phase detector logic signal flow graph

To achieve the transfer function of Fig. 11, a logic signal flow graph shown in Fig. 12 is required. In Fig. 4, the forward sequence corresponds to the logic signal flow graph sequence of states 1, 2, 3, 4, 1. For the BPSK phase detector of Fig. 12, the forward input sequence corresponds to the 5, 2, 7, 4, 5 state sequence, shown in black in Fig. 12. The corresponding waveforms are shown in the top waveforms in Fig. 13 and are identical to those of figure 4.

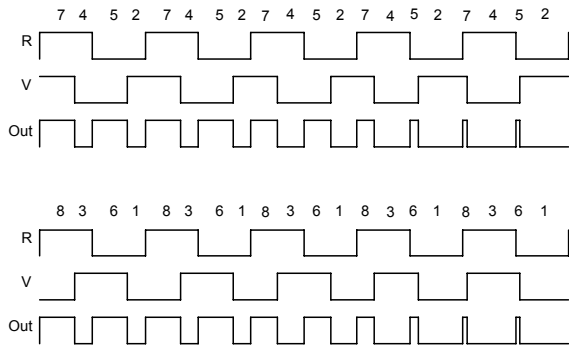


Figure 13. BPSK phase detector waveforms

When the BPSK data changes, a reverse input sequence shown in the bottom waveform of Fig. 13 results. This corresponds to the 1, 8, 3, 6, 1 sequence, shown in red on Fig. 12. The hardware design will result in a circuit with the block diagram of Fig. 14. Two feedback variables are required. From Fig. 12, it can be seen that it is not possible to include a Lock detection. It is however possible to include a BPSK data detection by detecting states 5, 2, 7, 4, 5 to correspond to a BPSK = 1 output and states 1, 8, 3, 6, 1 to correspond to a BPSK = 0 output.

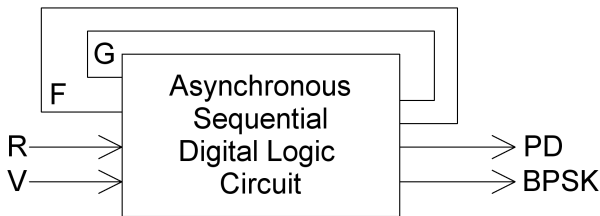


Figure 14. Hardware realisation of the BPSK phase detector.

The resulting ABEL equations for the circuit are:

$$\begin{aligned}
 F &= F \&V \# F \&R \# R \&V ; \\
 G &= G \&V \# G \&R \# R \&V ; \\
 PD &= F \$ G ; \\
 BPSK &= !R \&!V \&G \# !R \&V \&!F \# R \&V \&!G \# R \&!V \&F ;
 \end{aligned}$$

These equations were implemented in VHDL and applied to a CPLD for the realization. The waveforms of Fig. 13 can now be applied to the hardware to give the waveforms shown in Fig. 15. The waveforms on the left of figure 15, when BPSK = 1, are the same as those on the top of Fig. 13. The waveforms on the right, when BPSK = 0 are the same as those on the bottom of Fig. 13. The hardware performs thus exactly as required. The differences between the two phase detectors in this paper is highlighted by comparing Fig. 15 and Fig. 7, both have the same R and V input waveforms. When BPSK = 1, corresponding to a forward sequence, the PD waveform is the same, but when BPSK = 0, corresponding to a reverse sequence, the PD waveform is inverted. This is the PD output inversion required in the 180° to 360° region shown in Fig. 11 compared to Fig. 3.

Transitions between the forward and reverse sequences are implemented using the blue transitions in Fig. 12. They also result in the frequency detection capability shown in Fig. 16.

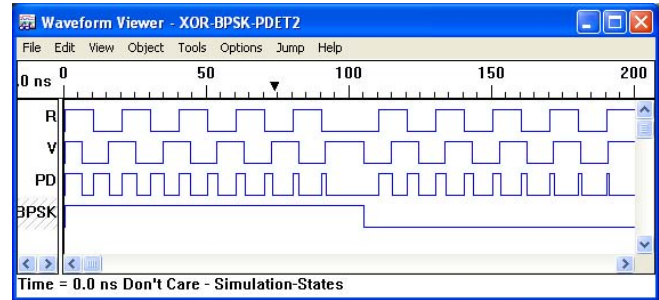


Figure 15. Hardware waveforms for the BPSK phase detector.

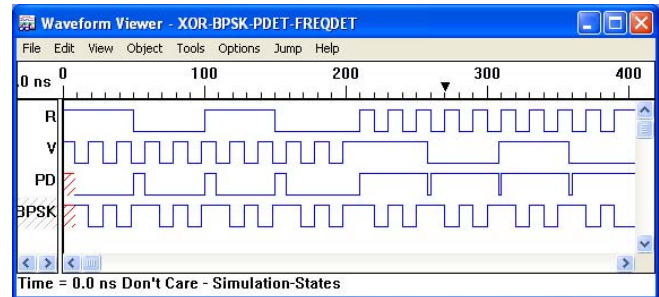


Figure 16. Frequency detection operation of the BPSK phase detector.

Using a typical CPLD or FPGA, allows these phase detectors to operate at input frequencies of several hundred MHz. For some devices, where a TTL like output rather than a CMOS like output drive capability is obtained, a complementary output, driving a differential analogue input to the loop-filter, will provide a linear output characteristic, corresponding to Figs. 3 or 11 as required.

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