

Frequency Shift Dither for Analogue to Digital Converters

Authors: Cornelis Jan Kikkert
Associate Professor
Head of Electrical and Computer Engineering
James Cook University
Townsville, Queensland, 4811
Phone 07-47814259
Fax 07-47251348
Email Keith.Kikkert@jcu.edu.au

Abbas Bigdeli
Electrical and Computer Engineering
James Cook University
Townsville, Queensland, 4811
Phone 07-47814867
Fax 07-47251348

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FREQUENCY SHIFT DITHER FOR ANALOGUE TO DIGITAL CONVERTERS

C. J. Kikkert and A. Bigdeli

James Cook University
Electrical and Computer Engineering
Townsville, Queensland, Australia, 4811
Email: Keith.Kikkert@jcu.edu.au, Abbas.Bigdeli@jcu.edu.au

ABSTRACT

This paper discusses a new dither technique to linearise an Analogue to Digital Converter (ADC). This typically results in a more than 20 dB reduction in harmonic distortion.

Additive dither [1,2,3,4] has been demonstrated to reduce the spuri to a significant extent. In this paper Frequency Shift (FS) dither is described. FS dither applies a frequency shift to the signals to be digitised. After Analogue to Digital conversion the signal is demodulated by removing this frequency shift using digital signal processing (DSP) techniques. FS dither has the advantage that the demodulated output has very low levels of harmonic distortion compared to a system without FS dither. By applying both Additive and FS dither at the same time, input signals with amplitudes far less than a quantum level can be digitised and detected accurately.

1. INTRODUCTION

Because of the lower cost, greater accuracy and reliability, many of the analogue signal processing operations in spectrum analysers, cathode ray oscilloscopes and radio receivers are being replaced with DSP techniques. The DSP techniques use an ADC to digitise the analogue signals. Practical ADCs suffer from limitations and unexpected side effects, which cause some harmonics, spurious components, quantisation noise and thermal noise to be added to the signal. The spuri and quantisation noise are due to the quantising nature of the ADC. These spuri are particularly noticeable if the spectrum of the sampled waveform is displayed. Such spectra are often used in measurements of communication systems, so that the reduction of spuri is of great importance. Depending on the relationship between the input frequency and the sampling frequency, the quantisation noise produced by the ADC process can occur at a limited number of frequencies only, resulting in significant spuri, which will limit the effectiveness of the ADC.

The cost and performance of an ADC for a given operating speed increases with the number of bits of the ADC. A 12 bit 30 MSPS ADC is about 8 times the price of a 10 bit ADC operating at the same sampling frequency. By reducing the spuri caused by the ADC, a 10 bit ADC can be used where otherwise a 12 bit ADC would be required, thus leading to significant cost savings. For sampling rates above

100 MSPS, only ADCs with 8 bits or less are generally available, so that the reduction of spuri is vital in order to obtain a good performance.

In order to investigate the behaviour of the ADC when different dither schemes are applied, their performance is normally simulated. Such a model must include:

- 1 The thermal noise due to the input circuitry of the ADC.
- 2 Random errors of the ladder network, due to manufacturing tolerances.
- 3 Amplitude related distortion.
- 4 Slew rate related distortion.
- 5 Slew rate related ladder network errors.

Figure 1 shows the simulated performance of an AD9050, 40 MSPS, 10 bit ADC. As shown in [4] the measured and computer simulated results show a very good agreement, with the measured SNR, Signal to Spurious ratio (SSR), Total Harmonic Distortion (THD) and SINAD being within 1 dB of the simulated values.

The level of spuri is very dependent on the input frequency used [4]. Both the simulation and the measurements show this dependency. There is a very close agreement between simulated and measured results, even for these nonlinear interactions. The ADC model can thus confidently be used to investigate other types of dither.

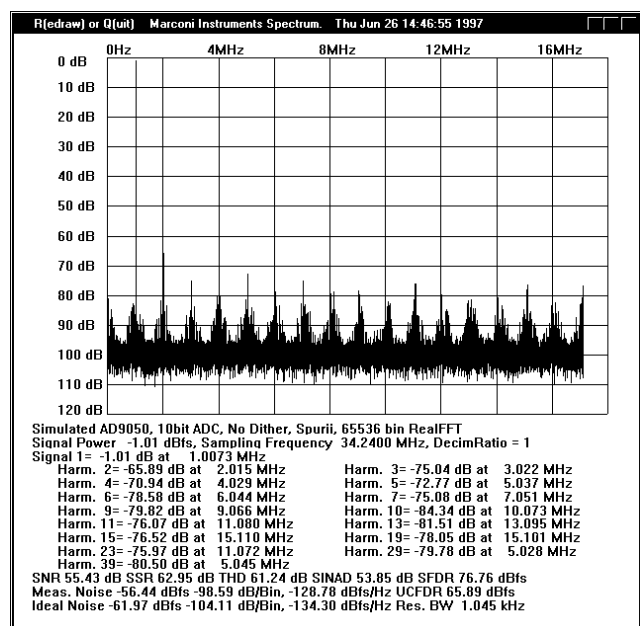


Figure 1. Simulated ADC 1.0073MHz input.

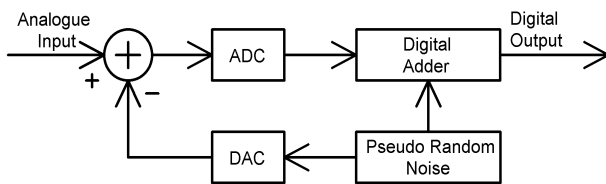


Figure 2. Additive Dither Block Diagram.

2. ADDITIVE DITHER

In a previous paper [4], the authors showed that the spuri can be reduced by adding noise and then subtracting this digitally. The block diagram of this system is shown in Figure 2.

A Pseudo Random Noise source is used to generate the noise. The propagation delay through the ADC must be allowed for by delaying the noise for the digital adder. The amplitude, sign and delay of the noise is adjusted carefully to achieve complete cancellation of the noise at the digital output. In the hardware realisation, a Lattice 2064 EPLD is programmed to contain the Pseudo Random Noise Generator, Noise Delay and the Digital Adder. Even though a 10 bit ADC is used, a 16 bit output is required from the digital adder, due to the noise having much finer quantisation steps.

Figure 3 shows the measured performance of the AD9050 ADC with additive dither. It can be seen that the signal to spurious ratio SSR has changed from 63.08 dB to 78.23 dB, a 15.15 dB improvement. The Unwanted Component Free Dynamic Range (UCFDR) is however not changed.

3. FREQUENCY SHIFT DITHER

It is possible to improve the performance of an ADC further by reducing the level of harmonics. This is achieved by frequency shifting the whole input spectrum prior to Analogue to Digital conversion and restoring the correct frequencies using digital signal processing techniques.

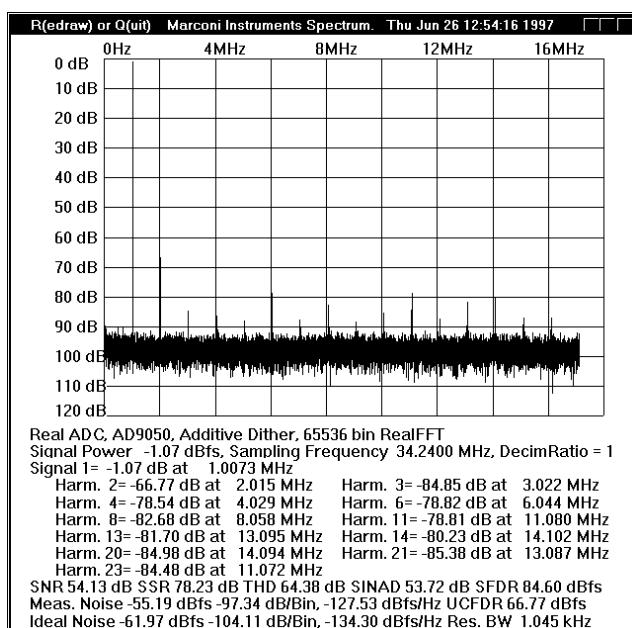


Figure 3. Measured ADC, Additive Dither.

In many spectrum analyser applications, the input signal is a high frequency signal and is progressively down-converted in the spectrum analyser. The frequency shifting required for FS dither can be accomplished by frequency modulating the last local oscillator prior to the ADC. In this paper we are considering a 40MSPS ADC operating at 34.24 MHz. Its Nyquist bandwidth is thus 17.12 MHz and such a spectrum analyser can usefully be used from DC to 15 MHz. If the last intermediate frequency (IF) is 70 MHz, with a ± 7.5 MHz bandwidth, then a 62.5MHz Local Oscillator is required to shift the spectrum to the DC - 15 MHz band. The block diagram required for this FS dither is shown in Figure 4. The low pass filter removes any high frequency components produced by the mixer and also serves as an anti-alias filter.

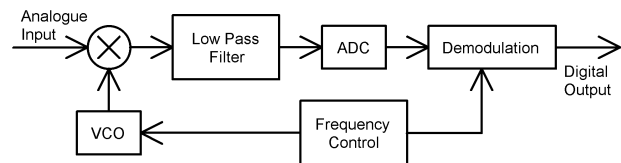


Figure 4. Frequency Shift Dither Block Diagram.

The VCO is now frequency modulated using the frequency control block shown in Figure 4. If a sinewave modulation with a 1MHz frequency deviation is applied to the VCO, then the whole input spectrum is shifted by this 1 MHz frequency modulation. Figure 5 shows the spectrum applied to the ADC for a 1 MHz sinewave input signal. Since the input spectrum to the ADC is frequency shifted, each component in the input spectrum becomes frequency modulated with the same frequency deviation. Any harmonics of these signals produced by the ADC will have a higher frequency deviation. The second harmonic will have twice the frequency deviation and the third harmonic will have three times the frequency deviation.

During the demodulation process, these harmonics will be shifted back by the original frequency shift only, so that there will be a resulting frequency modulation to the

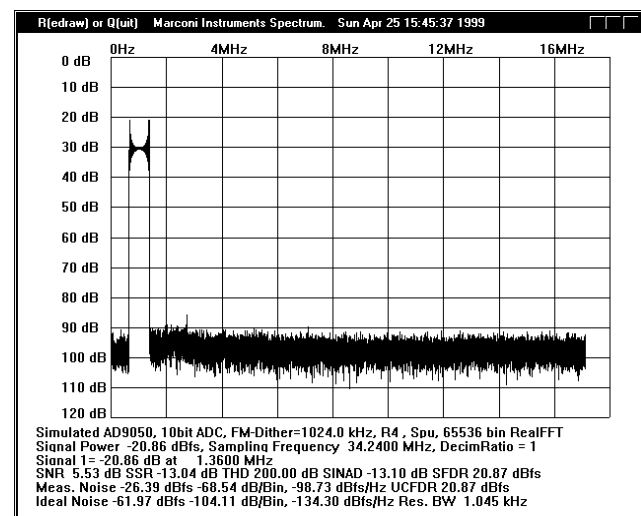


Figure 5. Modulated Input to the ADC.

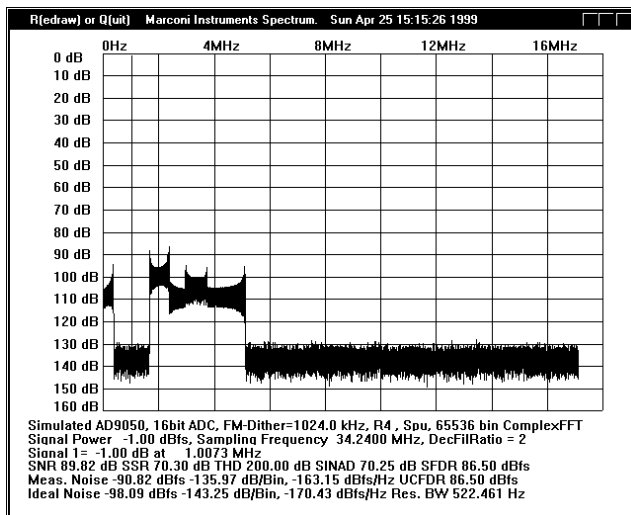


Figure 6. Demodulated Spectrum, 16 Bit Simulation.

harmonics produced by the ADC. Since the energy of the harmonics is now spread over a wide spectrum, the peak amplitude of each of the spectral components associated with each harmonics will be smaller and their spectrum will be more noise like. Figure 6 shows the spectrum corresponding to Figure 5 after demodulation. To show this effect, a 16-bit simulation is applied to the model of the 10 bit AD9050 ADC, thus reducing the quantisation noise produced by the model. The frequency deviation of the second harmonic distortion can clearly be seen. The third harmonic and fourth harmonic distortion is masked by aliasing of their spectra. Figure 7 shows the corresponding 10-bit simulation. The second harmonic distortion can only just be seen.

Comparing this spectrum with that of Figure 1, shows the significant improvement in the output spectrum. The Unwanted Component Free Dynamic Range (UCFDR) has increased from 65.89 to 87.45 dB. The largest unwanted component is the second harmonic and that has thus been reduced by 21.56 dB. A further increase in UCFDR can be achieved by increasing the frequency deviation. Since the spectral components caused by the ADC harmonics are now

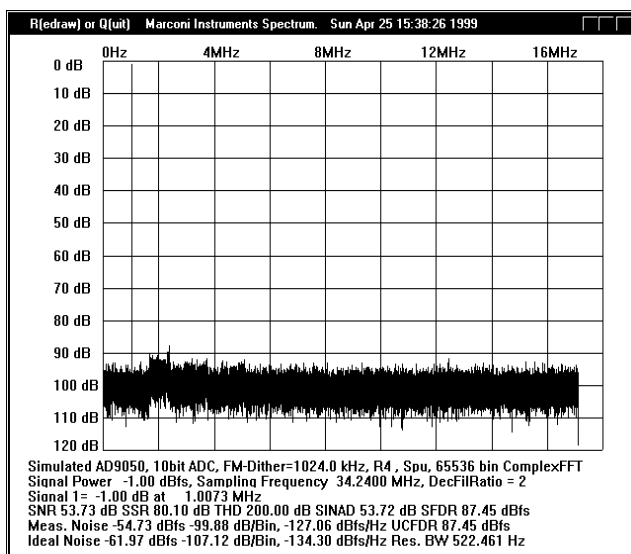


Figure 7. Demodulated Spectrum, 10 Bit Simulation.

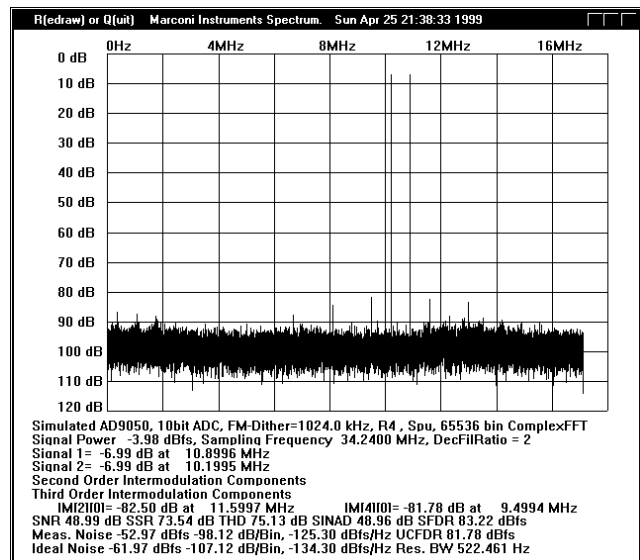


Figure 8. Two Tone Simulation with FS Dither.

noise like, they are reduced by 3dB when the number of samples used and its corresponding length of the FFT are doubled, as the noise per FFT bin is halved as its length is doubled.

The intermodulation (IM) distortion components will also have different frequency deviations applied to them. Some of the frequency deviations will match the input frequency deviation. For example the third order intermodulation components produced by $\pm 3f_1 \pm 2f_2$ will have the same frequency deviation as the input signal. As a result their amplitude will not be suppressed by the FS dither. FS dither does however suppress most of the intermodulation components as shown in Figure 8.

The corresponding two tone spectrum without dither has a Signal to Spurious Ratio (SSR) of 59.59 dB compared with 73.54 dB when FS dither is applied. Similarly, the UCFDR of 69.03 dB is improved to 81.78 dB and the THD of 58.75 dB is improved to 75.13 dB by applying FS dither. These are all significant improvements. Third order IM components are troublesome in most measurement systems and unfortunately FS dither does not eliminate them.

4. FS PLUS ADDITIVE DITHER

Additive dither has been shown [4] to greatly improve the performance of the ADC when subject to small input signals. For signals of more than 10 dB below full scale, no IM components can be detected when using additive dither. FS dither causes a great improvement in performance for large signals. By applying FS dither and additive dither, the ADC will give a very good performance for both large and small signals. As the input level decreases, the harmonics, which are masked by the FS dither will decrease further. For signals of more than 10 dB below full scale, no harmonics or IM distortion can be detected. Signals as low as -80dBfs, one tenth of a quantum level, can easily and accurately be detected using a 10 bit ADC with Additive FS dither. The block diagram for such a system is shown in figure 9.

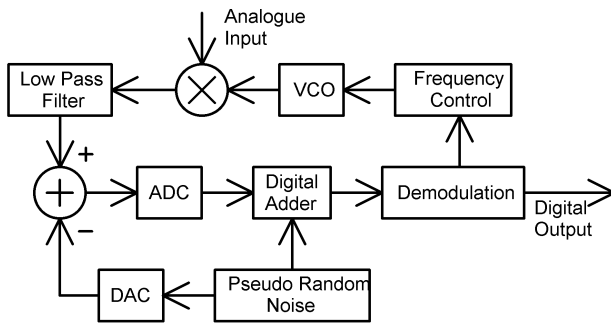


Figure 9. FS plus Additive Dither Block Diagram.

5. HARDWARE PERFORMANCE

Figure 9 shows that in order to improve the performance of the ADC, a significant amount of additional hardware is required. The signal degradation caused by that hardware should be less than the ADC performance as indicated by the computer simulations of Figure 7 and 8, otherwise the benefit of additive or FS dither is negated.

Additive dither can meet those requirements, as shown in Figure 3. In order to realise FS dither, an accurate VCO is required. This VCO must be able to be controlled in a precise manner, such that the resulting frequency modulation can be removed using DSP techniques after digitising.

A conventional analogue VCO cannot be used as the typical distortion to the modulated signal produced by an FM modulator is higher than the levels we are trying to cancel.

Commercial DDS IC's use 10 bit Digital to Analogue Converters (DAC) as part of their output stage. These produce a similar level of quantisation noise, spuri and distortion as the ADC one is trying to improve. The output from the DDS can be filtered, to remove some of the quantisation noise and spuri. Since the local oscillator required only has to cover $62.5 \text{ MHz} \pm 500\text{kHz}$, for the frequencies used to describe figure 4, a narrow band-pass filter can be used. This filtering can also be done using a phase locked loop (PLL), where the DDS is used for a frequency reference.

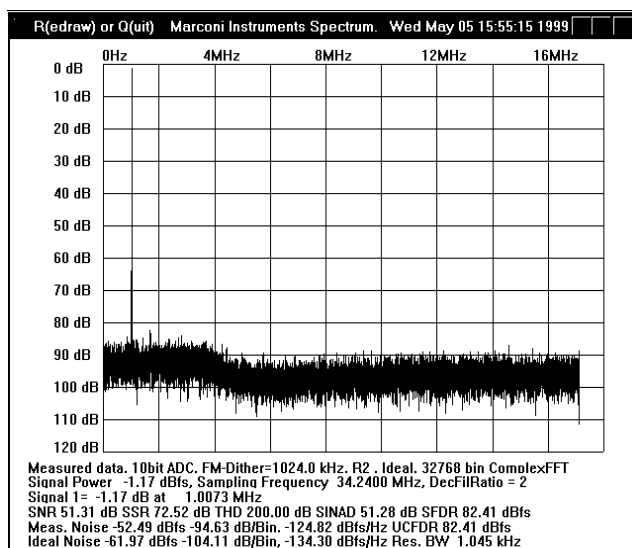


Figure 10. Measured ADC, FS Dither

Since the required local oscillator waveform is known precisely, one can also produce this waveform by playing a series of stored digital samples. The number of samples must be the same as the number of samples used in the FFT calculations. A 16 bit wide DAC should give a lower level of spuri and quantisation noise than a 10 bit ADC and can thus be used. Since at present such a system cannot economically operate at the required 62.5 MHz, the principles of operation of FS dither are demonstrated by generating the frequency shifted spectrum, like that in figure 5 directly, using stored digital samples driving a 16 bit DAC at 34.24 MSPS.

The resulting waveform is then used as input to the ADC. The resulting demodulated spectrum is shown in figure 10. It should be noted that the FFT length of figure 10 is half that of the other figures in this paper, due to limitations in our hardware. The raised noise level below 4 MHz is due to the quantisation noise produced by the 16 bit DAC. The output from the DAC is filtered with a 4 MHz cut off filter, resulting in an apparent quantisation noise reduction above 4 MHz. Comparing this spectrum with that of figures 1 and 7, the benefit of FS dither on a real ADC can be seen. The UCFDR has gone from 65.89 dB to 82.41 dB.

6. CONCLUSION

Computer simulations show that FS dither has the potential to greatly improve the performance of ADCs by virtually eliminating harmonic distortion produced by the ADC. The technique can be applied to any ADC. At present hardware limitations of the VCO required in the realisation prevent its full potential to be reached. This situation will change in the future with the introduction of better DDS signal sources.

7. ACKNOWLEDGEMENT

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