REDUCING DISTORTION IN MICROWAVE ANALOGUE TO DIGITAL CONVERTERS

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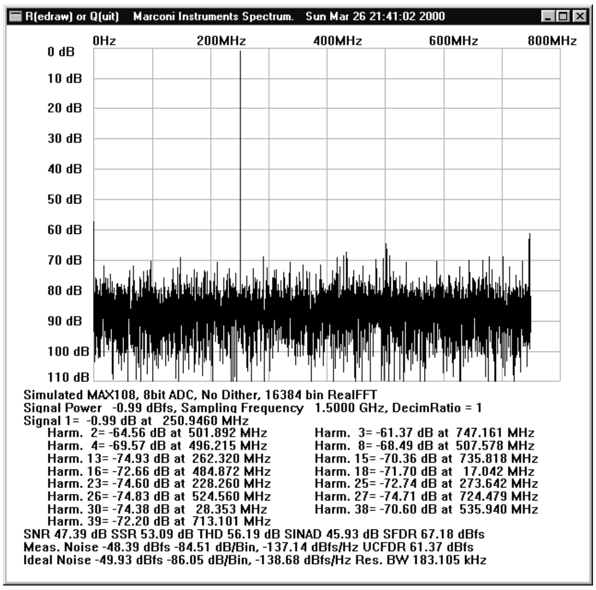
It is now possible to digitise microwave signals using 8 bit ADCs and sampling frequencies in excess of 1 GHz. This opens up new opportunities for the measurement and analysis of these broadband signals, however an 8 bit ADC has a very limited dynamic range. This paper discusses Additive Dither and Frequency Shift Dither techniques which can be used to extend the dynamic range of the ADC and it describes how this can be implemented in hardware.

1 Introduction

Because of the lower cost, greater accuracy and reliability, many of the analogue signal processing operations in spectrum analysers, cathode ray oscilloscopes and microwave receivers are being replaced with Digital Signal Processing techniques. An ADC is used to digitise the analogue signals and DSP techniques are used to perform the required signal manipulation. Practical ADCs suffer from limitations and unexpected side effects, which cause some harmonics, spurious components, quantisation noise and thermal noise to be added to the signal. The spurii and quantisation noise are due to the quantising nature of the ADC. These spurii are particularly noticeable if the spectrum of the sampled waveform is displayed. Such spectra are often used in measurements of communication systems, so that the reduction of spurii is of great importance. Depending on the relationship between the input frequency and the sampling frequency, the level of spurii produced by the ADC process can vary dramatically as shown in Fig. 1 and 2. These spurii limit the dynamic range of the ADC.

For many Microwave applications, bandwidths of several hundreds of MHz are required. For sampling rates above 200 MHz, only ADCs with 8 bits or less are generally available [1], so that the reduction of spurii is vital in order to obtain a good performance. To investigate different techniques for reducing spurii, the behaviour of the ADC is simulated. The ADC model must include:



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Simulated MAX108, 8bit ADC, No Dither, 16384 bin RealFFT
Signal Power   -0.99 dBfs, Sampling Frequency   1.5000 GHz, DecimRatio = 1
Signal 1=  -0.99 dB at   250.9460 MHz
      Harm.  2= -64.56 dB at  501.892 MHz          Harm.  3= -61.37 dB at  747.161 MHz
      Harm.  4= -69.57 dB at  496.215 MHz          Harm.  8= -68.49 dB at  507.578 MHz
      Harm. 13= -74.93 dB at  262.320 MHz          Harm. 15= -70.36 dB at  735.818 MHz
      Harm. 16= -72.66 dB at  484.872 MHz          Harm. 18= -71.70 dB at   17.042 MHz
      Harm. 23= -74.60 dB at  228.260 MHz          Harm. 25= -72.74 dB at  273.642 MHz
      Harm. 26= -74.83 dB at  524.560 MHz          Harm. 27= -74.71 dB at  724.479 MHz
      Harm. 30= -74.38 dB at   28.353 MHz          Harm. 38= -70.60 dB at  535.940 MHz
      Harm. 39= -72.20 dB at  713.101 MHz
SNR 47.39 dB SSR 53.09 dB THD 56.19 dB SINAD 45.93 dB SFDR 67.18 dBfs
Meas. Noise -48.39 dBfs -84.51 dB/Bin, -137.14 dBfs/Hz UCFDR 61.37 dBfs
Ideal Noise -49.93 dBfs -86.05 dB/Bin, -138.68 dBfs/Hz Res. BW 183.105 kHz
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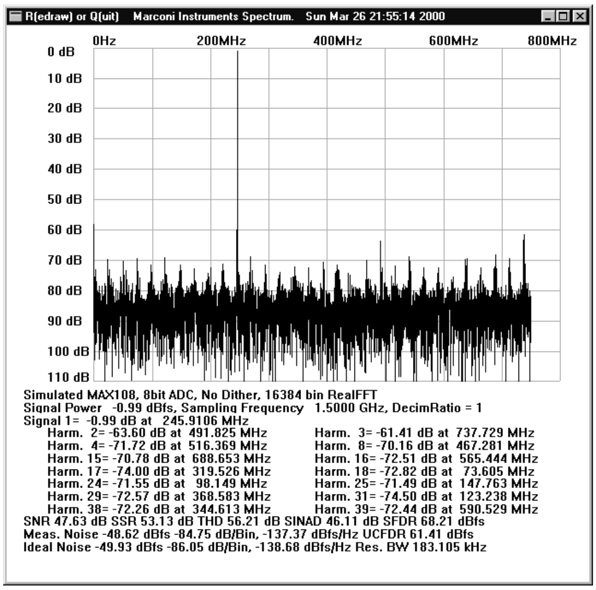
Fig. 1: 1.5 GSPS ADC, 250.946 MHz input.



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Simulated MAX108, 8bit ADC, No Dither, 16384 bin RealFFT
Signal Power   -0.99 dBfs, Sampling Frequency   1.5000 GHz, DecimRatio = 1
Signal 1=  -0.99 dB at   245.9106 MHz
      Harm.  2= -63.60 dB at  491.825 MHz          Harm.  3= -61.41 dB at  737.729 MHz
      Harm.  4= -71.72 dB at  516.369 MHz          Harm.  8= -70.16 dB at  467.281 MHz
      Harm. 15= -70.78 dB at  688.653 MHz          Harm. 16= -72.51 dB at  565.444 MHz
      Harm. 17= -74.00 dB at  319.526 MHz          Harm. 18= -72.82 dB at   73.605 MHz
      Harm. 24= -71.55 dB at   98.149 MHz          Harm. 25= -71.49 dB at  147.763 MHz
      Harm. 29= -72.57 dB at  368.583 MHz          Harm. 31= -74.50 dB at  123.238 MHz
      Harm. 38= -72.26 dB at  344.613 MHz          Harm. 39= -72.44 dB at  590.529 MHz
SNR 47.63 dB SSR 53.13 dB THD 56.21 dB SINAD 46.11 dB SFDR 68.21 dBfs
Meas. Noise -48.62 dBfs -84.75 dB/Bin, -137.37 dBfs/Hz UCFDR 61.41 dBfs
Ideal Noise -49.93 dBfs -86.05 dB/Bin, -138.68 dBfs/Hz Res. BW 183.105 kHz
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Fig. 2: 1.5 GSPS ADC, 245.91 MHz input.

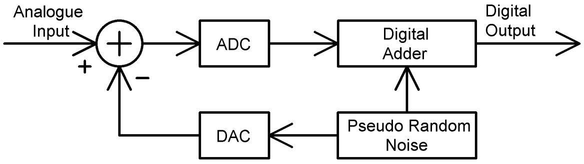
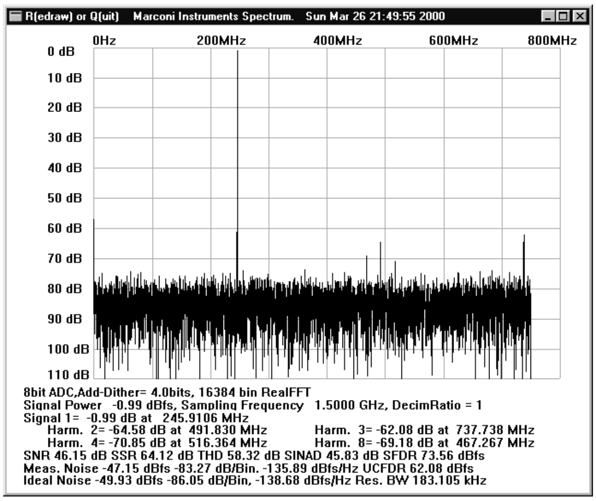


Fig. 3: Additive Dither Block Diagram.

1 The thermal noise due to the input circuitry of the ADC.
2 Random errors of the ladder network, due to manufacturing tolerances.
3 Amplitude related distortion.
4 Slew rate related distortion.
5 Slew rate related ladder network errors.



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8bit ADC,Add-Dither= 4.0bits, 16384 bin RealFFT
Signal Power   -0.99 dBfs, Sampling Frequency   1.5000 GHz, DecimRatio = 1
Signal 1=  -0.99 dB at   245.9106 MHz
    Harm.  2= -64.58 dB at  491.830 MHz          Harm.  3= -62.08 dB at  737.738 MHz
    Harm.  4= -70.85 dB at  516.364 MHz          Harm.  8= -69.18 dB at  467.267 MHz
SNR 46.15 dB SSR 64.12 dB THD 58.32 dB SINAD 45.83 dB SFDR 73.56 dBfs
Meas. Noise -47.15 dBfs -83.27 dB/Bin. -135.89 dBfs/Hz UCFDR 62.08 dBfs
Ideal Noise -49.93 dBfs -86.05 dB/Bin, -138.68 dBfs/Hz Res. BW 183.105 kHz
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Fig. 4: Additive Dither, 245.91 MHz Input.

Fig. 1 shows the simulated performance of a MAX108, at 1.5 GSPS, 8 bit ADC. These simulated results agree within 1 dB with the measured SNR, Signal to Spurious ratio (SSR) and Total Harmonic Distortion (THD) as shown in the data-sheet [2]. It should be noted that Maxim use only the first 5 harmonics for calculating the THD, while more than 30 harmonics are used in our simulation. Maxim also use a different definition for SINAD, the authors use SINAD as the ratio of the signal to the noise, spurii and distortion.

2 Additive Dither

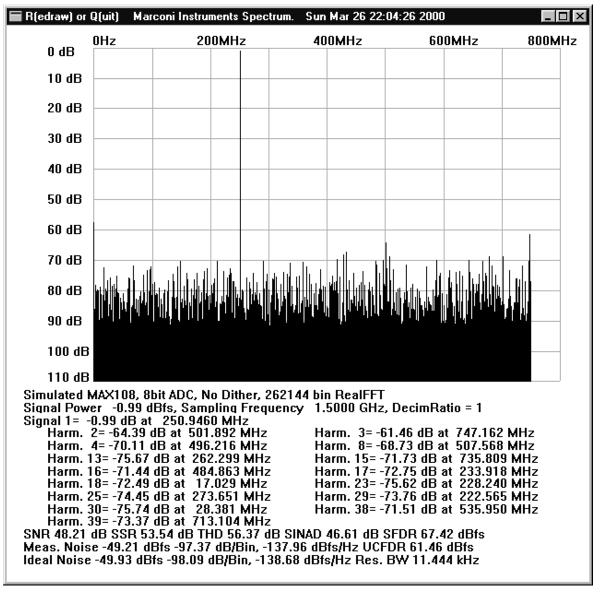
Adding low level noise [3] improves the "linearity" of the ADC. Additive Dither [4-5] is realised by adding pseudo random noise to the input of the ADC and then subtracting this digitally after the ADConversion. The block diagram of this system is shown in Fig. 3.

A Pseudo Random Noise source is used to generate the noise. The propagation delay through the ADC must be allowed for by delaying the noise for the digital adder. The amplitude, sign and delay of the noise is adjusted carefully to achieve complete cancellation of the noise at the digital output.

Figure 4 shows the simulated performance of the MAX108 with additive dither. It can be seen that compared with Fig. 2, the signal to spurious ratio (SSR) has improved by 11.0 dB. The harmonics and the Unwanted Component Free Dynamic Range (UCFDR) are however hardly changed. With Additive Dither the variation in performance with input frequency is radically reduced and virtually the same performance is obtained as the input frequency is varied. Additive Dither also results in a reduced level of spurii and a much improved amplitude accuracy for low input signal amplitudes.

3 Frequency Shift Dither

In many microwave measurement applications, the input signal is progressively down-converted to a frequency and bandwidth that can be handled by an ADC. The resulting digital data is then processed to obtain the required information, like a spectrum, transfer function, modulation properties etc. In this paper we are considering an ADC operating at 1.5 GSPS. Its Nyquist bandwidth is thus 750 MHz and such an ADC can be used to analyse data from DC to about 600 MHz. By frequency modulating the last local oscillator prior to the ADC, the whole input spectrum to the ADC is shifted in frequency. This is called Frequency Shift Dither [6]. If a sinewave modulation with a 12.5 MHz frequency deviation is applied to the VCO, then any second harmonic distortion produced by the ADC will have a 25 MHz frequency deviation, the third harmonic distortion will have 37.5 MHz deviation and so on. After the ADConversion, the initial frequency modulation is removed using digital signal processing techniques. Since only the 12.5 MHz frequency deviation of the input signal is removed, the second harmonic distortion will still have a 12.5 MHz frequency deviation and the third harmonic will still have a 25 MHz deviation. Since the energy of these harmonics is now spread over a wide spectrum, the peak amplitude of each of the spectral components associated with each harmonics will be smaller and their spectrum will be more noise like.



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Simulated MAX108, 8bit ADC, No Dither, 262144 bin RealFFT
Signal Power   -0.99 dBfs, Sampling Frequency   1.5000 GHz, DecimRatio = 1
Signal 1=  -0.99 dB at   250.9460 MHz
    Harm.  2= -64.39 dB at  501.892 MHz          Harm.  3= -61.46 dB at  747.162 MHz
    Harm.  4= -70.11 dB at  496.216 MHz          Harm.  8= -68.73 dB at  507.568 MHz
    Harm. 13= -75.67 dB at  262.299 MHz          Harm. 15= -71.73 dB at  735.809 MHz
    Harm. 16= -71.44 dB at  484.863 MHz          Harm. 17= -72.75 dB at  233.918 MHz
    Harm. 18= -72.49 dB at   17.029 MHz          Harm. 23= -75.62 dB at  228.240 MHz
    Harm. 25= -74.45 dB at  273.651 MHz          Harm. 29= -73.76 dB at  222.565 MHz
    Harm. 30= -75.74 dB at   28.381 MHz          Harm. 38= -71.51 dB at  535.950 MHz
    Harm. 39= -73.37 dB at  713.104 MHz
SNR 48.21 dB SSR 53.54 dB THD 56.37 dB SINAD 46.61 dB SFDR 67.42 dBfs
Meas. Noise -49.21 dBfs -97.37 dB/Bin, -137.96 dBfs/Hz UCFDR 61.46 dBfs
Ideal Noise -49.93 dBfs -98.09 dB/Bin, -138.68 dBfs/Hz Res. BW 11.444 kHz
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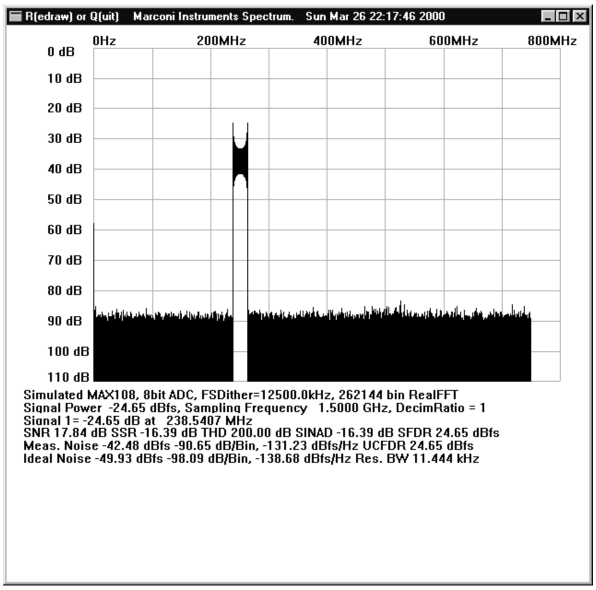
Fig. 5: Simulated ADC long FFT.



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Simulated MAX108, 8bit ADC, FSDither=12500.0kHz, 262144 bin RealFFT
Signal Power  -24.65 dBfs, Sampling Frequency   1.5000 GHz, DecimRatio = 1
Signal 1= -24.65 dB at   238.5407 MHz
SNR 17.84 dB SSR -16.39 dB THD 200.00 dB SINAD -16.39 dB SFDR 24.65 dBfs
Meas. Noise -42.48 dBfs -90.65 dB/Bin, -131.23 dBfs/Hz UCFDR 24.65 dBfs
Ideal Noise -49.93 dBfs -98.09 dB/Bin, -138.68 dBfs/Hz Res. BW 11.444 kHz
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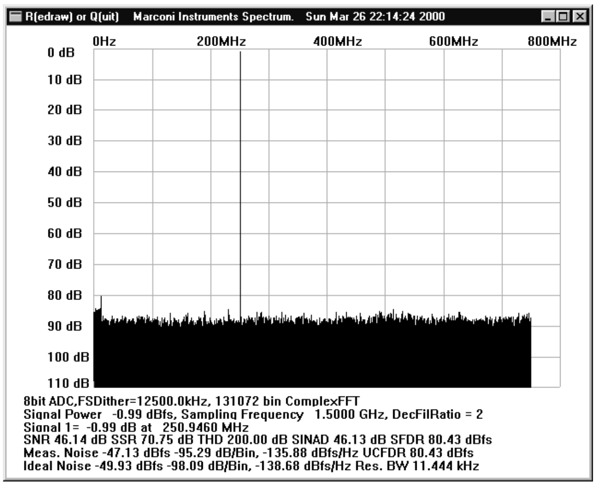
Fig. 6: Modulated Input to the ADC.

Fig. 5 shows the performance of the ADC without dither. This corresponds to Fig. 1 except a longer FFT has been used. Fig. 6 shows the frequency modulated input as it is applied to the ADC. Notice there has been a 23.6 dB reduction in the peak signal component. That same reduction will apply to the second harmonic distortion produced by the ADC. Fig. 7 shows the spectrum after demodulation. The frequency modulated spectrum of the second harmonic components have a peak amplitude of about -86 dBfs and can just be seen. The Unwanted Component Free Dynamic Range (UCFDR) is increased by 19.0 dB, compared with Fig. 5. The largest unwanted component at -80.43 dBfs is due to the DC component at the ADC output being frequency modulated during the demodulation process. A further increase in UCFDR can be achieved by removing this DC component at the output of the ADC, before demodulation, and by increasing the frequency deviation. Since the spectral components caused by the ADC harmonics are now noise like, they are reduced by 3 dB when the length of the FFT is doubled, as the noise per FFT bin is halved as its length is doubled.



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8bit ADC,FSDither=12500.0kHz, 131072 bin ComplexFFT
Signal Power   -0.99 dBfs, Sampling Frequency   1.5000 GHz, DecFilRatio = 2
Signal 1=  -0.99 dB at   250.9460 MHz
SNR 46.14 dB SSR 70.75 dB THD 200.00 dB SINAD 46.13 dB SFDR 80.43 dBfs
Meas. Noise -47.13 dBfs -95.29 dB/Bin, -135.88 dBfs/Hz UCFDR 80.43 dBfs
Ideal Noise -49.93 dBfs -98.09 dB/Bin, -138.68 dBfs/Hz Res. BW 11.444 kHz
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Fig. 7: Demodulated Spectrum, 8 bit FS Dither.

Most intermodulation (IM) distortion components will be reduced by FS Dither. However, third order intermodulation components produced by $\pm 3f_1 \pm 2f_2$ will have the same frequency deviation as the input signal. As a result their amplitude will not be suppressed by the FS dither. For a two tone input at -7 dBm, the third order IM obtained from simulation is -67.7 dBfs, compared with the -66.8 dBfs specified in the data sheet. Applying FS dither results in third order IM components of -69.6 dB.

4 Frequency Shift Plus Additive Dither

Additive dither makes the ADC behave in a more linear manner at low signal levels. FS dither results in a great reduction of spurii and harmonics. By applying Frequency Shift and Additive Dither, the ADC will give a very good performance for both large and small signals. Third order IM components will reduce by 3 dB for every 1 dB reduction in input amplitude. For two tone signals, each more than 13 dB below full scale, IM distortion is less than -83 dBfs. Signals as low as -80 dBfs, 30 dB below of a quantum level, can easily and accurately be detected using a 8 bit ADC with Additive FS dither.

5 Hardware Considerations

Fig. 8 shows the significant amount of additional hardware, required to implement both Additive and FS Dither. To have a net benefit, the signal degradation caused by this hardware should be less than the performance improvement due to Additive or FS dither.

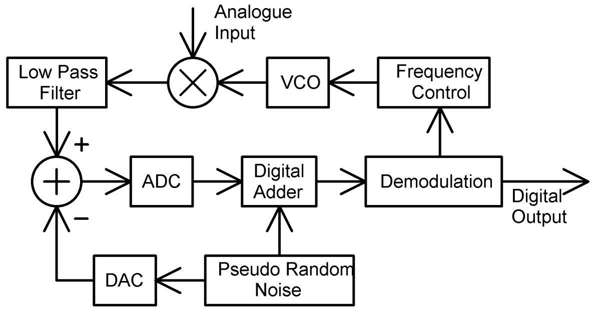

Fig. 8: Additive FS Dither Hardware Block Diagram.

Additive dither can readily be implemented with only a small performance degradation compared to the simulation [5]. In order to realise FS dither, an accurate VCO is required. This VCO must be able to be controlled in a precise manner, such that the resulting frequency modulation can be removed using DSP techniques after digitising. A conventional analogue VCO cannot be used as the typical distortion to the modulated signal produced by an FM modulator is higher than the levels one is trying to cancel.

The required FM signal can be produced by playing a series of stored digital samples or using Direct Digital Synthesis (DDS) and using a DAC to convert this into a frequency modulated sinewave. Since such a DAC will also generate spurii, this waveform cannot be used directly, but can be filtered using a PLL, where the DAC output is used for the frequency reference of the PLL. Using the PLL as a frequency multiplier allows a frequency modulated waveform, with a much smaller frequency deviation to be used. For example, a 2.5 GHz frequency modulated LO, can be produced from a 9.7656 MHz DDS output using a PLL with an 8 bit frequency divider (divide by 256). The DDS will thus need to have a 48.8 kHz frequency deviation to produce the final 12.5 MHz frequency deviation used in Fig. 7. The low pass filter in Fig. 8 should be designed to not introduce a non-linear group delay. It is not easy to meet all these requirements.

Additive FS dither has the potential to greatly improve the performance of ADCs by virtually eliminating harmonic distortion and spurii produced by the ADC. The technique can be applied to any ADC. At present the complexity of the hardware realisation of the VCO required prevent its full potential to be reached. This should change with the introduction of better DDS signal sources.

Acknowledgments

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References

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