

# A Satellite Beacon Receiver using Digital Signal Processing Techniques

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This paper describes the use of Digital Signal Processing techniques to Digitise and detect a beacon signal from a satellite. These techniques result in a cheaper Satellite Beacon Receiver, with an improved dynamic range and faster acquisition time.

## 1. Introduction

In the design of satellite communication links knowledge of the magnitude of the attenuation and depolarisation of signals at the desired frequency is a prerequisite. Attenuation of the satellite signals due to rain is very significant for frequencies above 5 GHz. As the spectrum becomes more crowded, operators are forced to use higher and higher frequencies. To enable the higher frequency bands to be used economically, the probability of a communication channel being not available due to rain, in a particular climate and for a particular link margin needs to be known. The most effective technique used to measure rain attenuation is experimentally monitoring the received signal strength of a satellite beacon. A satellite beacon is a low power signal transmitted for the purposes of up-link power control, telemetry and research. A beacon signal may be modulated but commonly it is not. The attraction of satellite beacons for propagation research is their constant signal strength. To measure the attenuation due to rain all that is required is to determine the beacon signal strength.

Due to the small power of most satellite beacons it can be difficult to measure rain attenuation with sufficient dynamic range. This paper describes the use of digital signal processing techniques to improve the performance a satellite beacon receiver over its analogue counterpart.

The authors have been involved in microwave propagation research for many years. As part of this research an analogue Ku band beacon receiver was developed [1]. A simplified block diagram of the analogue receiver is shown in Figure 1. The satellite receiver takes a 12.75 GHz beacon signal and a received power level of 1.5 fW (-118 dBm). The Beacon Receiver uses seven successive frequency shifting and amplification operations, in the converter blocks of Figure 1, to place the beacon signal at the centre of the final IF filter which is centred at 3.1818 kHz. The 12.75 GHz Low Noise Converter of Figure 1 uses a dielectric resonator oscillator for its local oscillator. These dielectric resonators will drift with temperature. A 500 kHz variation in frequency with a 30 K variation in temperature is typical. In this beacon receiver the low noise converter is

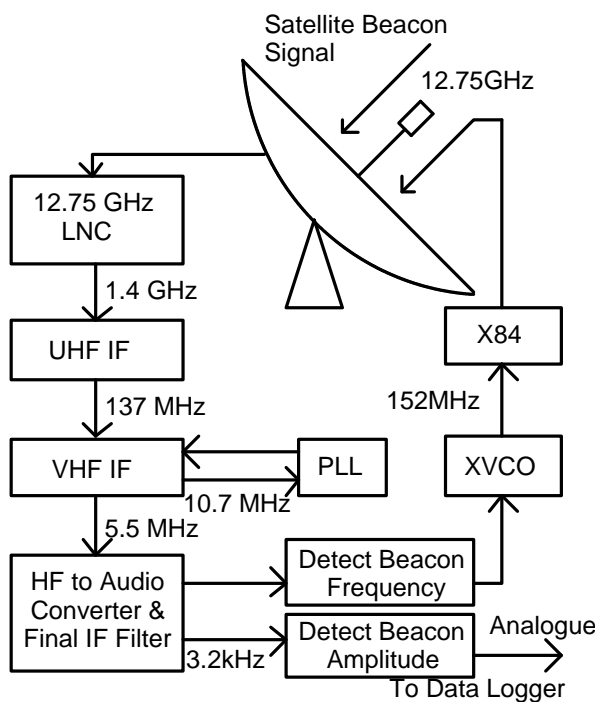


Figure 1. Old Beacon Receiver Block Diagram.

mounted at the focal point of a 3 m parabolic dish, the temperatures at that focal point can be quite high during the day and quite low at night. The frequency variation can be limited to less than  $\pm 100$  kHz by placing the down converter in an oven in order to keep its temperature constant or by using a much more expensive Crystal locked Low Noise Converter.

Because the received signal is so small, an IF bandwidth of less than 100 Hz is required in order to obtain a dynamic range of more than 35 dB. The down converted beacon signal should thus be within 50 Hz of the final IF filter centre frequency or within 0.005 parts per million of the carrier frequency. This frequency stability is far stricter than can be obtained with either the dielectric resonator oscillators used in the down converter or standard crystal oscillators. In addition a  $\pm 100$  kHz per annum drift of the satellite beacon frequency must be allowed for. Frequency control must thus be used in order to compensate for these frequency variations.

The frequency control for the beacon receiver consists of injecting a signal 5.2 MHz above the 12.75 GHz beacon signal into the receiver dish. The down conversion process places this injected signal at 10.7 MHz and the beacon at 5.5 MHz. The injected signal is then used in a Phase Locked Loop to cancel the drift due to the dielectric oscillator. A frequency locked loop controls the spacing between the injected signal and the beacon signal to ensure that the beacon signal is placed exactly at the centre of the 3.18 kHz final IF filter.

The injected signal and all the local oscillators used in the down conversion process must have a very low phase noise otherwise most of the beacon signal will spread outside the 100 Hz bandwidth of the 3.18 kHz final IF filter. VHF Voltage controlled crystal oscillators are used in the design to provide the low phase noise. Since each crystal is slightly different, a significant amount of alignment is required in order to ensure that the oscillators operate at the correct frequency and the resulting phase and frequency locked loops are stable.

These beacon receivers have been used successfully by various researchers in several propagation experiments. It was desired to improve the performance and decrease the manufacturing effort and therefore cost of future systems.

## 2. Digital Down Conversion

A new approach was devised using Digital Signal Processing techniques to replace the last two down conversion stages and the frequency control. The beacon signal at the 5.5 MHz IF frequency is digitised using reasonably priced Analogue to Digital Converters. In this application an Analog Devices AD9040 10 bit 40 MSPS Analogue to Digital Converter (ADC) is used to digitise the 5.5 MHz IF beacon signal. The 5.5 MHz IF filter used in the receiver has a typical bandwidth of 170 kHz. Sampling a 5.5 MHz signal requires a sampling frequency of at least 11 MSPS.

In the analogue hardware the 5.5 MHz signal is shifted in frequency and filtered. The same process is followed in the DSP hardware. A zero frequency intermediate frequency can be used and different positive and negative components can be identified if both In-phase (I) and Quadrature (Q) components are produced in the digital down conversion process. This then allows, decimation filtering to be applied, thereby reducing the IF bandwidth and reducing the data throughput. Decimation filtering also improves the signal to noise ratio. A block diagram of the digital down conversion process is shown in Figure 2.

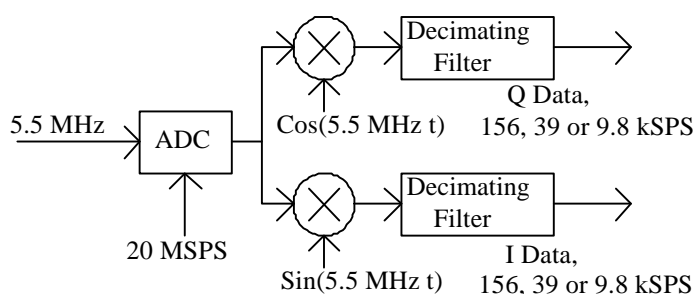


Figure 2. Digital Down Conversion Block Diagram

Harris Semiconductor make a Digital Down Converter (DDC) integrated circuit, the HSP50016, which includes the numeric oscillators for performing the down conversion and decimating filters for both the I and Q signals. The I and Q data is output as a serial data stream. All the elements shown in Figure 2 except for the ADC are included in the DDC IC, it can therefore be used as the basis for a cost effective solution in the beacon receiver.

An Analog Devices ADSP-2181 EZ-KIT Lite development board is used to control the Harris Semiconductor Digital Down Conversion IC HSP50016 and to perform the numerical processing tasks. This development board has two serial ports, one which is used for communicating with a PC which is used for logging the output data, the other is used for controlling and receiving the I and Q data from the Harris Semiconductor HSP50016. Both serial ports are synchronous but RS-232C communication to the PC is achieved using a software UART.

### 3. Implementation

The beacon signal at the input of the digital hardware is confined to a 200 kHz band centred at 5.5 MHz, due to a TV Sound IF filter being used prior to the ADC. The sampling rate must be at least 11 MHz so a rate of 20 MHz was chosen. This is sufficiently high and it is not a multiple of 5.5 MHz to avoid harmonic problems. The ADSP-2181 communicates with the DDC via a synchronous serial port. The functions of the DDC are set by transmitting 40 bit control words. Since one serial port is used to both control the DDC and receive data some special measures had to be taken. At power-up the ADSP-2181 serial port clock is used to provide the DDC control data clock. This allows transmission of the initial control words to set the modes of the DDC and start the DDC serial clock at the correct frequency. When the DDC serial clock is running it is then used as the serial clock for sending control data to the HSP50016 and receiving I and Q data using the ADSP-2181 serial port. The clock hand-over is done by on-board logic under processor control.

At start-up the signal must be located inside the 200 kHz bandwidth. The DDC decimation is initially set to 512, which produces a useable output bandwidth of about 20 kHz. Therefore to cover the 200 kHz band ten adjoining search bands are required. The frequency of the DDC is set to the centre of the lowest band and 1024 I and Q values are sent serially to the ADSP-2181. A fourth order Blackman-Harris window is applied to the data then a 1024 point Radix-4 decimation-in-frequency FFT is performed. A peak detection algorithm is applied and the magnitude and frequency of the largest signal is stored. The process is repeated for the remaining nine bands. When this is complete the largest signal in all of the bands is chosen. The reason behind examining all bands and not accepting the first large signal is that the beacon may be modulated and the system must not choose a sideband as the peak signal. During this first scan the resolution bandwidth is 38Hz/bin and the data rate is 39.06 kSPS. As the processing time is much smaller than the time required to obtain the data, it can be seen that this process is completed in a fraction of a second.

When the frequency of the peak signal has been determined the frequency of the DDC is set to match. At this point the decimation is changed to 2048. The output bandwidth is then about 4.8 kHz and the resolution 9.5 Hz/bin. The data rate is now 9.77 kSPS. The increase in decimation achieves a 33 dB increase in SNR and thus gives a significant improvement in the dynamic range of the system. The sampling commences at the new decimation rate and after windowing, the FFT and peak detection the magnitude of the peak signal is transmitted from a serial port on the DSP board as RS-232C data. This data is an ASCII string representing the magnitude in decibels. The measurement process repeats at about 8 Hz.

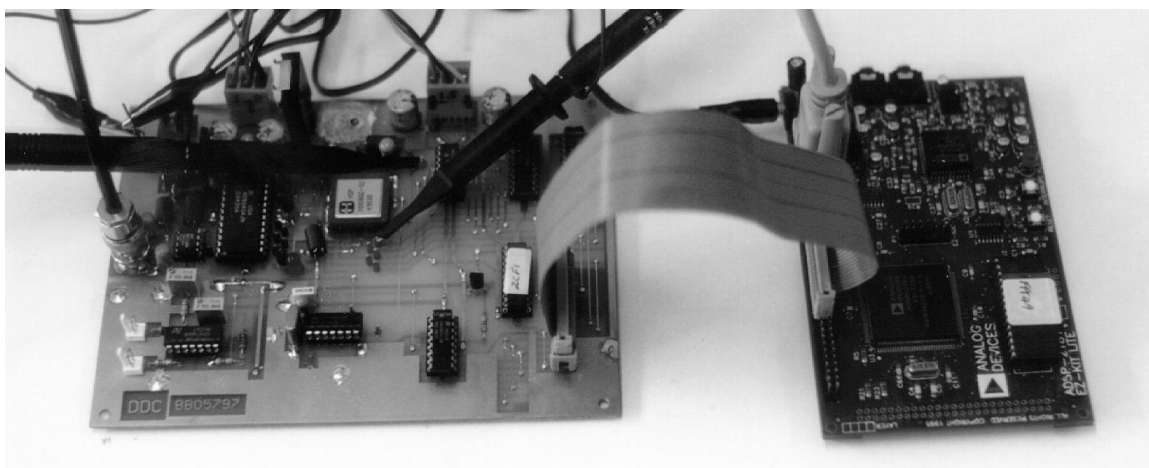


Figure 3. ADC, DDC and DSP Hardware

Figure 3 shows the resulting hardware. The board on the left contains preamplifiers, the AD9040 ADC, the HSP50016 and some logic. The board on the right is the ADSP-2181 development board used in the implementation.

The satellite beacon signal will drift in time and temperature variations of the Local Oscillators used in the Beacon receiver will also cause frequency shifts of the beacon signal at the Analogue to Digital Converter input frequency of 5.5 MHz. As a consequence, a tracking algorithm must be implemented. When the detected peak is outside the centre third of the frequency spectrum of the FFT, a control signal is sent to the DDC to change its centre frequency to match that of the Beacon Signal. After each correction the signal is thus located in the centre of the output band. This ensures that the signal is always well within the output bandwidth. These changes are made with virtually no change in output data rate.

When a signal fade occurs, the signal will drop and may disappear into the noise. If it does, the system will then wait 15 seconds for the signal to reappear before doing a wide search of the entire 200 kHz bandwidth. In a fade of short duration the probability of a significant frequency drift is small and the signal should return in the same frequency band. Since the wide search is fast (<0.1 s) the re-acquisition of the signal is almost immediate once it becomes slightly larger than the noise per bin.

In order to ensure that the system is locked to the largest signal and not a sideband or spurious component in another band a wide search is performed every minute. This guarantees that regardless of unforeseen circumstances, such as a large temporary interference from a local transmitter, the system is measuring the peak beacon signal at all times.

A significant part of the existing analogue beacon receiver hardware shown in Figure 1 is associated with the harmonic multiplication required to inject a signal into the dish at 5.2MHz (10.7MHz-5.5 MHz) above the beacon signal. This injected signal is required to compensate for the diurnal frequency variation of the 12.75 GHz LNC. The hardware required for this can be removed if the frequency of the Local oscillator used in the VHF IF strip is controlled directly by the DSP board. If the injected signal is no longer used, the 5.5 MHz beacon signal can have a frequency variation of  $\pm 0.5$  MHz, placing it well outside the 5.5 MHz IF filter bandwidth. The first step in finding the beacon signal must thus be a frequency sweep of the VHF VCO in order to place the Beacon signal somewhere near the centre of the 5.5 MHz IF band. That is done by setting the DC control signal for the VCO and using a 512 decimation ratio, detecting the presence of a beacon signal. If no signal is detected, the control voltage is changed and the process repeated. Once the Beacon Signal is within  $\pm 25$  kHz of 5.5 MHz, the DDC frequency is varied to place the down converted beacon signal at DC, which is the centre of the zero IF frequency used in the Digital Down Conversion.

When the beacon signal drifts, the DDC frequency is varied first, as described above, until the beacon is more than 50 kHz from 5.5 MHz. Then the VHF VCO is controlled until the beacon again is within  $\pm 25$  kHz of 5.5 MHz. Large drifts of the Local Oscillators used in the Beacon Receiver can thus be accommodated.

The resulting block diagram of the system is shown in Figure 4. By comparing it with Figure 1, it can be seen that a significant

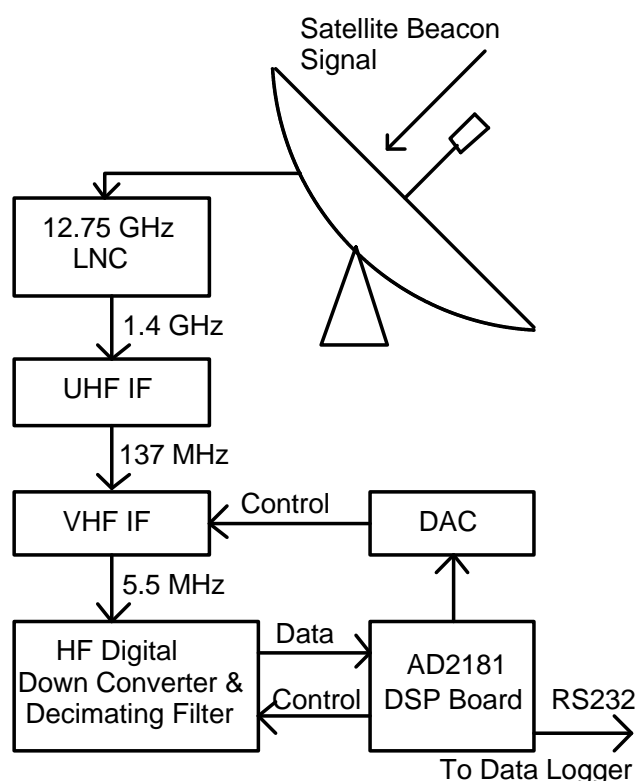
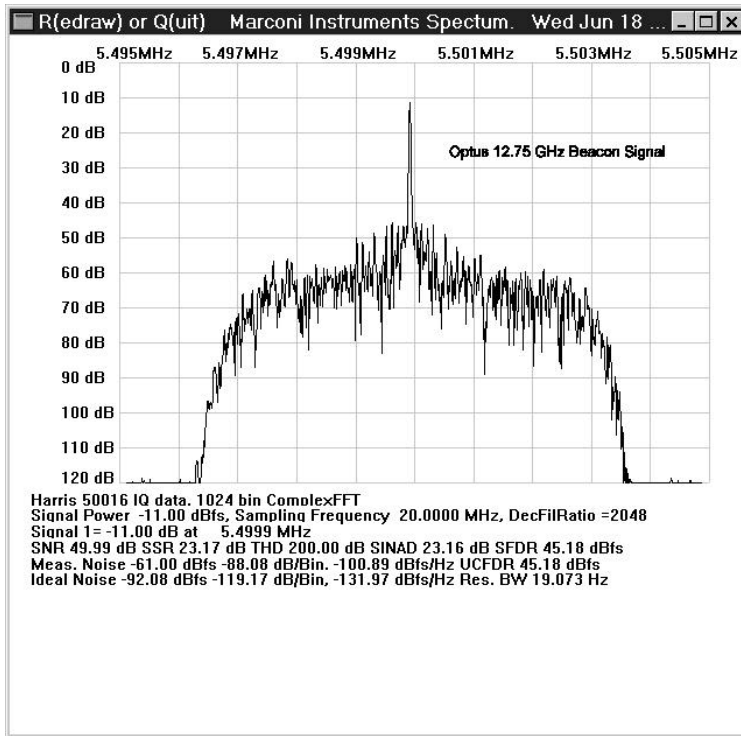


Figure 4 New Beacon Receiver Block Diagram.



**Figure 5. Received Beacon Signal.**

amount of analogue hardware has been eliminated, thus reducing the cost.

#### 4. Performance

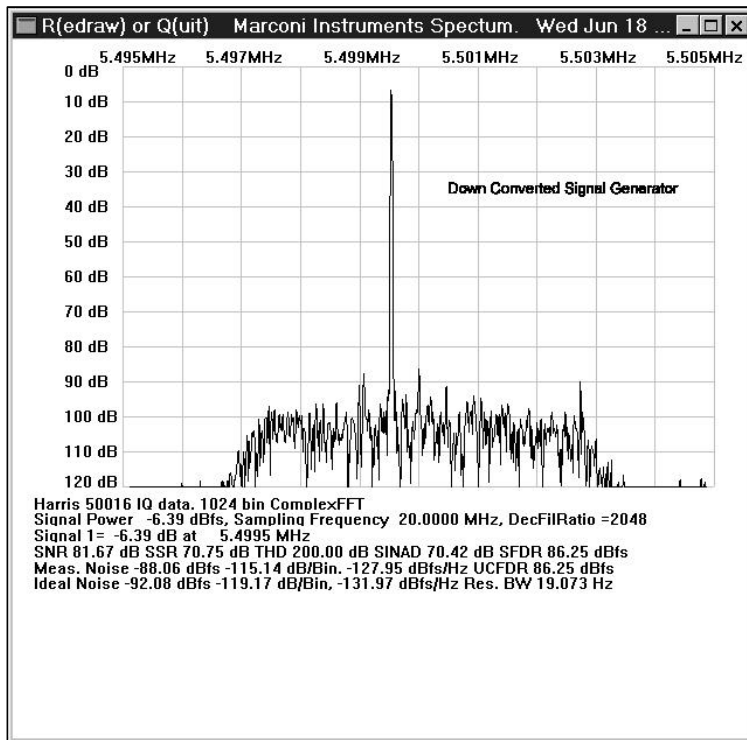
Figure 5 shows the actual output spectrum of a 12.75 GHz Optus Satellite beacon after being detected using the DDC described in this paper. A very small amount of 100Hz frequency modulation of the spectrum can be observed. That is due to Frequency modulation of the Local Oscillators used in the beacon receiver, caused by 50 Hz mains ripple on power supplies. The amount of frequency modulation is less than 0.1 Hz frequency deviation. It should be noted that the 5.5 MHz IF signal has a substantial amount of noise. That noise is thermal and radiated noise and represent a noise figure of about 1.4 dB, for the whole beacon receiver. In order to prevent any overload to the ADC, due to the noise, the signal level must be kept small. A 10 bit ADC will

however have sufficient dynamic range to allow the beacon signal to be digitised in the presence of the noise.

The new system provides many advantages over the previous analogue system:

- 1 The receiver will acquire the beacon very quickly and reliably. The 1 MHz wide VCO control sweep is performed within a few seconds. Once the signal is within the 5.5 MHz IF band, the time to acquire or re-acquire the signal is a fraction of a second. A wide search using the DDC can be performed in less than half a second compared to about a minute for the analogue sweep used in the analogue system of Figure 1.
- 2 The beacon receiver now has the intelligence to pick the carrier of a modulated beacon or a beacon that is close to other signal components. That is very difficult to do using analogue electronics.
- 3 The signal detection is done using a FFT. This allows very narrow bandwidths to be used, thereby increasing the dynamic range and enabling the beacon signal to be tracked through deep fades where other beacon receivers would loose lock.
- 4 There are few critical components, large diurnal temperature drifts of Local Oscillators can be allowed for. This means that the adjustments and alignment required during production is minimised. The cost of production of the Beacon Receiver has thus been improved by the elimination of much of the time-consuming tuning of the analogue hardware.

By generating the same amount of noise as is obtained using the actual beacon signal and setting a signal generator amplitude and frequency to match that of the beacon signal after down conversion to 5.5 MHz, the performance of the DDC system can be evaluated. These tests did not incorporate the UHF VCO frequency control. The observed test spectrum is thus exactly like that of Figure 5. The receiver's ability to track frequency changes and the accuracy of tracking changes in amplitude can easily be investigated by varying the amplitude or frequency of the signal generator. These tests indicated that the beacon receiver will remain locked for fades in excess of 40 dB and that the beacon receiver will regain lock when recovering from deeper fades at close to the 40 dB fade depth. The detected fade accuracy was within the  $\pm 0.5$  dB calibration accuracy of the signal generator and the precision attenuators used to vary the signal amplitude. No matter what amplitude and frequency changes were tried the beacon receiver always regained lock immediately the signal frequency was within  $\pm 100$  kHz of the required 5.5 MHz and a few dB above the noise level.



**Figure 6. Down Converted 5 MHz sinewave.**

beacon acquisition and a larger dynamic that a conventional analogue beacon receiver. Due to the built in intelligence of the DSP detection system, the beacon receiver is able to lock onto the carrier of a modulated beacon.

These DSP techniques can be applied to produce beacon receivers at other frequencies, provided suitable low noise converters are available.

## 6 Acknowledgment

This work was partially supported by ARC Large Grant A49531784, and the authors gratefully acknowledge their support.

## 7 References

- 1 Kikkert C. J. "The Design of a 12 GHz Narrowband Low Noise Receiver" 1992 Asia-Pacific Microwave Conference, Adelaide, August 1992, pp 809-812
- 2 Kikkert C. J., B. Bowthorpe, G. H. Allen, "Satellite Beacon Receiver Improvement using Digital Signal Processing, ISSPA '96, Gold Coast, Australia, August 1996, pp 517-520

The dynamic range of the DDC system can be demonstrated by simply using a signal generator without adding any noise as is described above. Decimation by 2048 increases the dynamic range by 33 dB, resulting in a 92 dB signal to noise ratio in an ideal 10 bit ADC. Figure 6 shows the spectrum that is obtained under these conditions. The measured noise is 4 dB worse than the ideal performance. The measured noise is -115 dBfs per bin, indicating a close to 100 dB dynamic range. By comparing Figure 6 and Figure 5 it can clearly be seen that the noise in Figure 5 is not due to the digital down conversion system.

## 5 Conclusion

Digital Down Conversion can be applied successfully to a satellite

beacon receiver. The resulting system is cheaper to produce and has a faster