

## SUBJECT OUTLINE

# **CC2510 Digital Logic and Computing Methods**

(Teaching Period 1, 2009)

Campus: **Townsville** and Mode of Offering: **On Campus**

### **HANDBOOK DESCRIPTION:**

CC2510 - Digital Logic and Computing Methods, 3 Units, Student Contribution Band: 2. Administered by the Discipline of Electrical & Computer Engineering.

Prerequisites: EG1002 or CP1300

65 hours lectures, tutorials, demonstrations and practicals, site visits and/or seminars.

**Section A: Digital Logic** Boolean algebra and minimisation, practical design of combinational and clocked synchronous sequential logic circuits; ABEL representation of digital logic; programmable logic devices and programming these devices, logic families and interfacing.

**Section B: Computing Methods** programming engineering applications in structured programming tools and environments.

### **Learning Objectives**

- Section A: Digital Logic translate an English based requirements statement into a form suitable for implementing as a logic design;
- Section B: Computing Methods a detailed knowledge of the management principles of multi-module software design and development;
- demonstrate an ability to describe the electrical properties of, and justifiably select between, the commonly used logic family technologies, including EPLD devices;
- design minimum gate count combinational logic circuits;
- design synchronous sequential logic to satisfy state machine requirements;
- develop a top-down programming style using structured programming techniques applied to a common programming language and operating system for the development of maintainable applications from a design specification;
- discuss, in a cohesive and valid manner, the design processes and selection criteria used in digital logic design;
- write ABEL programs to realise combinational and sequential logic circuits.

### **GENERIC SKILLS TO BE FOSTERED:**

#### **Literacy and Numeracy**

- the ability to read complex and demanding texts accurately, critically and insightfully
- the ability to speak and write clearly, coherently and creatively
- the ability to generate, calculate, interpret and communicate numerical information in ways appropriate to a given discipline or discourse

#### **Information Literacy**

- the ability to find and access information using appropriate media and technologies
- the ability to evaluate that information

- the ability to select and organise information and communicate it accurately, cogently, coherently, creatively and ethically
- the ability to deploy critically evaluated information to practical ends

### **Critical Thinking and Problem Solving**

- The ability to think critically, to analyse and evaluate claims, evidence and arguments, and to reason and deploy evidence clearly and logically
- The ability to adapt knowledge to new situations
- The ability to deploy critically evaluated information to practical ends
- The ability to define and to solve problems in Digital Logic and Computing Methods

### **Self Reliance and Interpersonal Understanding**

- The ability to lead, manage and contribute effectively to teams
- the ability to work individually and independently

### **Using Tools and Technologies**

- the ability to select and use appropriate tools and technologies
- the ability to use online technologies effectively and ethically

### **Learning Achievement**

- the acquisition of coherent and disciplined sets of skills, knowledge, values and professional ethics from at least one discipline area
- the ability to reflect on and evaluate learning, and to learn independently in a self directed manner
- the ability to manage future career and personal development

### **GRADUATE QUALITIES TO BE FOSTERED:**

- exemplary personal and professional moral and ethical standards
- a commitment to life long learning and intellectual development
- an understanding of regional issues
- a sense of professional, community and environmental responsibilities

### **STAFF:**

<b>Lecturer</b>	<b>Room #</b>	<b>Consultations</b>	<b>Email contact</b>	<b>Telephone</b>
<b>A/Prof. Keith Kikkert</b>	<b>DD014-111</b>	Monday 10-1 Friday 9-10:30	<b>Keith.Kikkert@jcu.edu.au</b>	<b>4781 4259</b>

### **CLASS TIMES:**

The nominal lecture, tutorial and practical times are given below. Because of other commitments, there may be some modifications to this schedule. If this occurs, details will be provided by the lecturer during class.

#### **CC2510 Lecture Timetable 2009**

Week	Date	Tuesday 10am	Thursday 3pm	Thursday 4pm	Friday 2pm	Friday 3pm	Friday 4pm
1	23-Feb-09	L					
2	02-Mar-09		L	L	L	T	
3	09-Mar-09		L	L	L	L	T
4	16-Mar-09	T	L	L	L	L	T
5	23-Mar-09	T	L	L	L	L	
6	30-Mar-09						
7	06-Apr-09		L	L	Good Friday	Good Friday	Good Friday
8	13-Apr-09	T	L	L	L	L	
Recess	20-Apr-09	Recess	Recess	Recess	Recess	Recess	Recess
9	27-Apr-09	T	L	L	L	L	T

10	04-May-09	T	L	L	L	L	T
11	11-May-09	T	L	L	L	T	
12	18-May-09	T	L	L	L	TR	
13	25-May-09	T	L	L	L	TR	

Practicals: Monday 9am to 12 noon. Practical do not meet each week. The schedule is available from the subject web site.

### ATTENDANCE REQUIREMENTS:

Attendance at all assigned class times is expected. While attendance at prescribed classes is not a component of assessment in any subject, the Head may allow participation in class activities to be an assessment component, provided that the criteria are made clear to students. There is a high correlation between non-attendance and failure in the subject. You are responsible for all information (both technical and administrative) presented during class times. You should establish informal study groups and one function of these is to give you access to information, if for any reason, you miss a class session.

Students repeating this subject must attend *all* scheduled sessions (lectures, tutorials, practicals, *etc.*), as though they were taking the subject for the first time.

### TEXT BOOK/S:

#### Prescribed Texts

*None*

#### Reference Texts and Journal Articles

John. F. Wakerly, Digital Design Principles and Practices, Fourth Edition, Prentice Hall 2005,

Douglas L. Perry, VHDL programming buy example, McGraw Hill, 4<sup>th</sup> ed. 2002.

*J. Basker VHDL Primer (3<sup>rd</sup> Ed)*, Prentice Hall, 1999

### EPLD PROGRAMMING RESOURCES:

Lattice EPLD programming software is used during this course. A CD with the Lattice Starter kit software is available and students are allowed to use that software on their own computers.

### TEACHING SUPPORT MATERIALS:

**Subject Web site:** LearnJCU available through Students *ONLINE* on the JCU web site via Current Students <https://www.jcu.edu.au/studentsonline/index.cfm> and [www.eng.jcu.edu.au/subjects/cc2510](http://www.eng.jcu.edu.au/subjects/cc2510) are both used. Lecture, tutorial, laboratory and resource information for this course will be available via the Web.

**E-mail:** The CC2510 email alias is activated so please read your email on a regular basis so as not to miss important notices.

### EXPECTED CLASS AND STUDY TIME:

The number of class hours in any one week will vary depending on the scheduling of practicals. There will be 3 hours of lectures and 1 or 2 hours of tutorials each week, the four practicals will require three hours each. A report on one practical session is to be written and there is one assignment. Self study outside of class periods will vary from student to student, but you should expect to spend *at least* 6 hours of study in addition to class time each week.

Closed footwear must be worn in room DD014-209. Please refer to the laboratory section in the subject web pages for full details of Laboratory safety requirements.

### ASSESSMENT:

For information on the award of grades, policy on supplementary and deferred examinations, see the School of Engineering web page <http://eng.jcu.edu.au/Current%20Students/policy/index.shtml>.

**A student must obtain at least an average of 40% over all invigilated components within a subject to pass the subject overall. Invigilated assessment is defined as that which can be solely attributed to the student (i.e. formal quizzes, examination, seminars).**

The assessment for this subject is comprised of the following components:

Component	Weighting
Assignments	20%
Practicals	15%
Tutorial Preparation	5%
End of Semester Examination (Invigilated)	60%

**Exam (60%).** A 2-hour examination in June will be worth 60% of the overall assessment. The primary emphasis will be to test that the student has an understanding of the material outlined in the course, can articulate this understanding and is able to apply this knowledge to solve engineering problems. **You must obtain at least 40% in this examination to pass the subject.**

**Tutorial Preparation (5%).** Some tutorials problems should be done by the student outside the tutorial periods, and the tutorials session are used to go through the solution of that problem. For some of these (selected at random) a mark will be given for the attempt done by the student.

**Assignment (20%).** An assignment which trains the student to gather and filter information and present the resulting filtered information in a written report appropriate for a particular audience.

Assessment of the assignment may take into account individual effort, achievement and reporting skills. Details are provided from the Assignment link on LearnJCU. Further information will be provided during class.

**Practicals (15%).** There are four laboratory sessions for this subject. The practicals require preparation, participation and *individual* reporting. One laboratory session will be written up as a full report and that will be worth 6%, the others will be marked in class and are worth 3% each. Guidelines for the preparation of reports, general lab procedures and safety requirements are available at the 2<sup>nd</sup> level practical sessions web site: <http://www.eng.jcu.edu.au/subjects/ece2labs/PracProcedures.pdf>.

**Note :** It is your responsibility to ensure you have a mark recorded before leaving the room when completing a practical that is to be assessed during the laboratory session.

Safety is a very important consideration during practicals. Please see *Safety Requirements for Engineering Buildings* on the School of Engineering web pages at <http://www.eng.jcu.edu.au/resources/studentinfo/.XXX>

#### **ASSESSMENT CRITERIA:**

The assessment criteria for the assignment is included in the assignment document. The criteria for the practicals are on the laboratory web site <http://www.eng.jcu.edu.au/subjects/ece2labs/PracProcedures.pdf>

#### **SUBMISSION OF ASSESSMENT:**

The practical reports should be submitted to the relevant pigeon hole in stairwell on the first floor of the Electrical Engineering Building DD014. The assignment must be submitted electronically as instructed in the relevant assignment guidelines, through safe assign in LearnJCU on or before the due date, to permit an automatic plagiarism check to be performed on your submission. Late submissions will be penalised at 5% per day or part thereof up to a maximum penalty of 50%. The marks awarded will be placed on the JCU web site. If you are unable to submit any piece assessment, you must seek the approval of the Subject Coordinator. Failing to do so will result in the awarding of an “RW” (*i.e.* Result Withheld) grade for the subject. The grade will remain an “RW” until such time that the outstanding items of assessment are submitted. Outstanding “RW” grades will be automatically converted to a grade of “N” (*i.e.* a failing grade) two weeks after the Publication of Results data. It is therefore in every student’s best interest to submit all items of assessment.

Students repeating this subject must submit all assessable material, as though they were taking the subject for the first time.

Students must check that the grades they receive on their returned on-course assessment items match the grades published by the Subject Coordinator on the subject web page. Any differences between the published and returned grade must be brought to the attention of the Subject Coordinator, so that the calculated grade reflects the true performance of the student.

Items of assessment *not* submitted will be published as DNS (*i.e.* did not submit). Students have until the last day of the Study Vacation to lodge a claim of submission for items granted a DNS. Note that items not submitted will trigger the “RW” rule, detailed above. The assessed work will be returned in lectures/tutorials or can be obtained from the lecturer’s offices.

### **PLAGIARISM:**

Plagiarism is the act of using another’s words, works or ideas from any source as one’s own. Plagiarism has no place in a University. Student work containing plagiarised material will be subject to disciplinary action and may result in exclusion from the University. The University Policy on Plagiarism may be found in the JCU Student Handbook towards the end of the section provided below:

[http://www.jcu.edu.au/td/topics/JCUPRD\\_016786.html](http://www.jcu.edu.au/td/topics/JCUPRD_016786.html)

Students should also be aware of the JCU policies relating to Student Academic Misconduct (cheating) found at [http://www.jcu.edu.au/policy/student/rights/JCUDEV\\_005375.html](http://www.jcu.edu.au/policy/student/rights/JCUDEV_005375.html) This website also gives help on avoiding plagiarism.

**The assignment submissions will be automatically checked for plagiarism. Plagiarise and you will be caught and the University procedures must then be followed.**

### **FINAL GRADE:**

The raw marks that you receive from each piece of assessable material will be combined into a total mark for the subject. These raw marks may undergo a scaling process to ensure meeting School and University policies on the distribution of grades. Please see *Assessment Policy* on the School of Engineering web pages at <http://eng.jcu.edu.au/Current%20Students/policy/index.shtml>.

### **DEFERRED EXAM:**

The award of a deferred examination is *not* automatic even if a valid medical excuse is presented. A request for a deferred examination may be refused if the student has a poor record of participation (e.g. failure to attend mandatory sessions, or failure to submit *all* assessable material). Please see *Deferred Assessment Policy* on the School of Engineering web pages at <http://eng.jcu.edu.au/Current%20Students/policy/index.shtml>.

### **WORKPLACE HEALTH AND SAFETY:**

The University staff, management and students have mutual obligations in relation to maintaining a safe workplace and learning environment. Students are required to follow directions specific to sites and safety procedures as directed by staff. Failure to follow safety instructions may result in that person being denied access to the facilities. Please see School of Engineering policy located at the following web site, <http://eng.jcu.edu.au/Current%20Students/policy/index.shtml>

### **STUDENT SUPPORT:**

Some students will have problems that can span a wide range of family, relationship, health, emotional, financial and educational issues. Both the School and University have support systems. We can help, but if problems occur you must seek help promptly. See your lecturer, the Associate Dean (Engineering), or contact Student Services via the web page <http://www.jcu.edu.au/student/>.

Teaching and Learning Development offer help with learning skills such as writing and referencing, preparing for exams, etc at <http://www.jcu.edu.au/learningskills/>

The library staff provide a range of support services for IT access and library issues <http://www.library.jcu.edu.au/InfoHelp/Training/>

### **STUDENTS WITH DISABILITIES:**

Students with a disability who require special arrangements or consideration should contact the Associate Dean (Engineering) and the Disability Resource Centre at <http://www.jcu.edu.au/office/disability/>.

## SYLLABUS:

<b>Introduction</b> .....	1 Lecture
<b>Combinational Logic Design Techniques</b> .....	4 Lectures
Truth Tables and Boolean Algebra Theorems	
Karnaugh Maps	
Logic Design procedure	
Quine McCluskey Algorithm	
<b>Introduction to Programming Logic Devices</b> .....	6 Lectures
Compilers and software	
ABEL: structure, equations, truth tables, test vectors	
Schematic Entry	
Examples	
<b>Sequential Logic</b> .....	4 Lectures
FlipFlops, Counters	
Synchronous Sequential Logic	
State Diagrams	
Design Examples	
<b>VHDL programming language</b> .....	11 Lectures
Language structure, Examples and hardware realisation	
Hardware Realisation, pin allocation	
VHDL programming for sequential logic, Design Examples	
<b>Documentation Standards</b> .....	1 Lecture
Circuit diagrams and Timing	
<b>Logic Functions</b> .....	1 Lecture
Decoders, Buffers and Encoders	
Multiplexers and Comparators	
<b>Logic Hardware</b> .....	3 Lectures
CMOS and TTL Logic	
Input and Output structures	
<b>Programmable Logic</b> .....	8 Lectures
Programmable Technologies	
PAL, EPROM, EPLD, FPGA Device Overview.	
Microprocessor and DSP realisation using FPGA's	
Current and future trends	