

James Cook University
Electrical and Computer Engineering
EE4305 Assignment

Introduction

This assignment is worth 20% of the total of the course and covers material given by A/Prof Kikkert and A/Prof Mazierska. The Electronics Design will be marked by appropriate parts of the assignment will be marked by A/Prof Kikkert and the EPLD realisation will be marked by A/Prof Mazierska.

The assignment is to be submitted by 5pm on the 5th of October. As a solution will be posted on the web on the 6th of October, late submissions will not be accepted.

Task

Design a circuit to have two inputs, A and B and at least two LED outputs. The circuit is to light one LED, or a sequence of LEDs if the frequency of input A is higher than that of input B and it is to light the other LED, or another sequence of LEDs if the frequency of input B is higher than the frequency of input A. The circuit is to operate reliably over a wide range of input frequencies. The design can be done using either synchronous or asynchronous logic techniques. The design should be your own work and publicly available designs, such as those published in hobby magazines will not be accepted. (These designs also do not satisfy all the requirements of this assignment).

This design is to be fitted into a Lattice ispLSI2032. The JCU-ECE EPLD development board will be used to verify your EPLD design. To facilitate testing, the input pins are to be I/O12 and I/O13 and the output pins are to include the LED outputs I/O17 and I/O18 and may include all the 8 LEDs connected to I/O 16-23 if needed.

This assignment will require much more "thinking time", to formulate the design strategy, than the time required to complete the actual design. The solution to be posted on the web is less than three pages of Logic Signal Flow Graphs, flow tables and Karnaugh maps.

C. J. Kikkert
26 Aug 98