

James Cook University
Electrical and Computer Engineering
EE4305 Assignment

Introduction

This assignment is worth 10% of the total of the course and covers material given by A/Prof Kikkert. The assignment is to be submitted by 5pm on the 25th of October.

All the Synario files will need to be provided, so that the design can be verified. The files required are all the files required to re-compile the design, as well as your jed files. To ensure that your files remain together put them into one Zip file and use a unique identifier, like your student ID as part of the name. Any new attachment with the same name as an existing one will simply overwrite the old one. If all the assignments sent were called 'assignment2' only the last one sent would exist in the attachment directory. Ensure that your design is labelled with your name. (ie in the module or schematic). A brief report describing the design is required.

Task

Design an asynchronous sequential circuit to read data from an Integrated Device Technology Inc. (www.itd.com) ITD7204 FIFO with a organisation. The (8 bit) output data from that FIFO are to be sent to a PC on it's parallel port. Details for the Centronics three-wire hand-shaking are on the CC3501 web site under John Nielsen's lectures and IBM pinwriter connections.

Your circuit is to read the FIFO and while it is doing so, keep the busy line high. When it has placed the data in the output buffer, the standard width acknowledge pulse is to be generated and the busy line is to go low, both indicating that valid data is available. The PC will then read that data and when it has finished doing so initiate a strobe pulse. That strobe pulse is to be detected by your circuit and result in the reading of the next data word from the FIFO. If the FIFO buffer is empty the circuit is to wait with busy high, until new data arrives in the FIFO.

This design is to be fitted into a Lattice ispLSI2032. The JCU-ECE EPLD development board will be used to verify your EPLD design.

For testing, the data output is to be connected to the DAC pins (IO0 to IO7, pin 15 to 22) of the JCU EPLD test board, with pin IO0, pin 22 being the least significant bit. The /strobe pin is to be pin 3, the busy pin is pin 4, the /acknowledge pin is pin 5, the FIFO /read is pin 6, the FIFO empty flag is pin 7, the FIFO retransmit is pin 8 and the data from the FIFO are to connect to pins 25 to 32 with pin 25 being the least significant bit.

This assignment will require much more "thinking time", to investigate the problem and to formulate the design strategy, than the time required to complete the actual design. The solution will be posted on the web shortly after the submission date.

C. J. Kikkert
21 Sept 99

