

James Cook University
Electrical and Computer Engineering
EE4306 Assignment

Introduction

This assignment is worth 10% of the total of the course and covers VHDL programming and Asynchronous Sequential Logic.

The assignment is to be submitted by 10am on the 11th of September.

Task

Design an Phase Locked Loop IC to include an Exclusive OR type Phase Frequency detector and a divide by N network to permit a VCO to be controlled in 1 kHz steps from 11.0 MHz to 11.25 MHz. Complete the design for the PLL circuit and program this into a Lattice ispLSI2032 using the JCU-ECE EPLD development board to verify your EPLD design and using the VHDL programming language.

The divider is controlled using jumpers connected to pins 25 to 32 of the EPLD board (pin 25 is the least significant bit of the control word). The LED on pin 37 is to be used to indicate an out of lock condition with the VCO being a higher frequency than the 1 kHz Reference Frequency and the LED on pin 38 is to indicate an out of lock condition with the VCO being a lower frequency than the 1 kHz Reference Frequency. The Phase detector output and its complement are to appear on pins 3 and 4 respectively.

Email your complete tested design, with the whole directory containing the Lattice Project Zipped as one file. Use a unique file name for this Zip file, as a file Assignment.Zip will overwrite another file of the same name when receiving an attachment. Ensure your name is included in the source code as well as in the file name sent.

The solution will be posted on the web shortly after the submission date.

C. J. Kikkert
21 Aug 00