

James Cook University

Electrical and Computer Engineering

EE4306 VHDL programming Assignment

Design a Noise Generator using VHDL programming techniques and the Lattice ispLSI2032 devices used on the EPLD board used in the labs. The pdf file of the schematic for that board is on the web under EE4306/labs. The noise generator is to consist of a 10 bit Pseudo Random noise source, a second and different Pseudo Random Noise Source and a four bit wide adder to produce 16 output values. The four bit wide adder is to add 4 bits from each of the Pseudo Random Sequences to produce the 16 near random output values, consisting of the 4 least significant bits of the adder. These outputs are connected to the 4 most significant bits of the 8-bit DAC on the EPLD board. No carry output is required from the adder. The VHDL code for this noise generator is to contain separate architectures for each of the Pseudo Random Generators and the adder. (In order to demonstrate the use of the combination of separate modules to provide the overall function.) The pin connections for the 8-bit DAC are pin 15 to pin 22 with pin 15 being the least significant bit and pin 22 the most significant bit. The clock input for the circuit is to be the normal clock input at pin 11.

The second Pseudo Random Noise Sequence is to be the longest that you can fit into the EPLD in conjunction with the 10-bit PR sequence and the 4-bit adder.

This Assignment, with the Lattice files on Floppy disk, should be submitted by email to Keith.Kikkert@jcu.edu.au, by Monday 10 September 5pm and will be worth 10% of the final mark for the subject. (Note that emailing the files, will give an automatic date stamp.) Please keep a copy of the Zip file as that will give further proof of your file dates in case of problems.

The submission should include the Project files, VHDL files, Waveform test files, JED files etc in electronic form. Ensure that your name is included in the VHDL files and project file. If emailing the files, ensure your file names include a unique identifier, like your computer account name as two files with the same name may overwrite each other in the mail system. To ensure that no files are lost, it is advisable to ZIP the complete project directory into one file (with a unique identifier) and email that file.

Testing of the assignment will be by loading the project files for this assignment into the Lattice Software. The marking will include a functional test by downloading the JED file supplied into one of the EPLD test boards, as well as evaluating the suitability of the VHDL code, verifying that the project was compiled (by checking the tick marks) and checking the test waveforms for both the adder and the noise generators. No paper copy need be provided.

It is suggested that you test your design by feeding the noise output from the EPLD board into the line input of a soundcard on a computer. The waveform should sound noise like and no repetition of the waveform should be noticed.

C. J. Kikkert
2 August 2001