

# James Cook University

## Electrical and Computer Engineering

### EE4306 VHDL Assignment

Occupational Therapy at James Cook University require a small alarm that will bleep to advise a wearer to record the activities/stance/task they are currently undertaking on a small diary. The evidence shows this is more effective at getting a sense of the things people do through a regular day than asking someone to record *all* activity in a diary for 24hrs or so. An assignment designing this was set for CC2510 during first semester.

A modification of this is set as a VHDL assignment for EE4306.

#### **The requirements are:**

The timer is to give a short beep (up to say 2-3 beeps in 3 secs) at a random point in every hour period. The system is to use a watch crystal for a clock (32768 Hz). The audible alarm is to be a piezoelectric speaker, this is to be driven directly from the CPLD in a differential manner. There is to be at least 5 random time checking intervals every minute.

#### **The Task is:**

Write the VHDL code for such a system. It is not necessary to construct any hardware, however the design should fit in either a ispLSI2032 PLCC package IC or an ispLSI2064 TQFP package IC. The clock should be connected to pin 11 and the differential timer outputs (to be directly connected to the piezoelectric speaker) are to be on pin 28 and pin 29.

Submit the complete design before 5pm on Monday 9 September. The assignment is worth 10% of the total course. Zip the complete directory for the VHDL code and all the resulting ispLever project files and email this to [Keith.Kikkert@jcu.edu.au](mailto:Keith.Kikkert@jcu.edu.au) , by the due date.

Ensure that all the submitted items (VHDL code included) are clearly labelled with your name and student number.

C. J. Kikkert  
12 August 2002