

James Cook University

Electrical and Computer Engineering

EE4306 VHDL Assignment

A cheap key-pad obtainable from Dick Smith Electronics or Jaycar is to be used together with a ispLSI2031 CPLD for an electronic lock.

The requirements for this lock are:

- 1 It must have at least 6 digit key code, ie 080903 is a suitable code
- 2 It must provide an output high when the door is to be opened. This logic level high then drives a door latch amplifier, whose design is not part of this assignment.
- 3 The lock is to have a Keypad reset or keypad clear, operated by the # key
- 4 It must provide a logic level high alarm output when three successive # key pressed have been made without a correct key code.
- 5 The correct key code clears the alarm counter and also turns off any alarm.
- 6 For the demo version only, the * key is to also clear the alarm counter and turn off the alarm.
- 7 Complementary outputs to drive a buzzer are to be provided. These use any suitable AC (clock derived) signal in a push-pull arrangement.
- 8 The master keycode must be able to be changed easily. The test master codes are 892003 (the assignment due date), or if your code cannot handle the two same keys in succession the code is 080903. If your design handles more than 6 digits, please specify the code used in your documentation.

The Aim:

The aim of this assignment is to:

- 1 Provide practice in VHDL programming, and in particular it provides practice at writing hardware efficient code.
- 2 Provide practice in problem formulation and problem solving skills.
- 3 Provide practice in code debugging and code optimisation to minimise the hardware resources required.

The Task is:

Write the VHDL code for such a system. Several JCU designed CPLD development boards containing an ispLSI2032 and fitted with keypads are available.

To make the required CPLD pin connections compatible with these test boards, you should use the following pin assignments:

The clock is connected to pin 11.

The Row scanning lines for the keypad are to be connected to pin 30 for the top row, pin 25 for the second row from the top, pin 26 for the third row from the top and pin 28 for the bottom row.

The Column scanning lines for the keypad are to be connected to pin 29 for the left column, pin 31 for the middle column and pin 27 for the right column.

The Door Open signal is to be connected to pin 3.

The Alarm signal is to be connected to pin 4.

The PBuzzer signal is to be connected to pin 5 and its complementary NBuzzer signal is to be connected to pin 6.

For verification of the design the length of correct keystrokes counter is to be connected to pins 44 to 41, with pin 41 being the least significant bit. (Note your design may not require all these counter bits).

You may include any other test signals you desire at the remaining pins.

Submit the complete design before 9am on Wednesday 10 September. The assignment is worth 10 marks being 10% of the total course. Zip the complete directory for the VHDL code and all the resulting ispLever project files and email this to Keith.Kikkert@jcu.edu.au , by the due date.

The marking scheme will include marks for how well the code is commented and documented.

Up to 3 marks will be given for comments and documentation

Up to 2.5 marks will be given for correctly functioning keypad scanning code.

Up to 2.5 marks will be given for correctly functioning keysequence marching code

Up to 2 marks will be given for fitting the design in the CPLD, **compiler ticks should be present in your zipped files.**

As a minimum requirement a fully functional, 6 digit key sequence electronic lock, which detects key presses only and thus cannot allow the same key to be used twice in succession is able to achieve full marks. For such a design 892003 will not work because of the 00. For these designs the test sequence is 090903.

Having a design that fits in the CPLD **and** detects both key presses and key releases and thus overcomes this limitation is awarded an extra up to 4 bonus marks. Those designs will be tested with the sequence 892003

As a minimum requirement the alarm is to be a simple logic level output. Having the PBuzzer and NBuzzer outputs working to produce an audible alarm **and** fitting in the CPLD is awarded an extra 1 bonus mark.

Making the sequence 8 digits long and fitting that in the CPLD is worth 1 bonus mark.

It is thus possible to obtain 16 marks for this assignment, which is worth 10 marks. However a considerable extra effort is required for this and the rewards are not just the bonus marks, but also a higher skill level.

Ensure that all the submitted items (VHDL code included) are clearly labelled with your name and student number.

Keypad information:



Connector information:

Keypad connections	1	2	3	4	5	6	7	8
Function	NC	Col1	Row0	Col0	Row3	Col2	Row2	Row1
CPLD pin number		31	30	29	28	27	26	25

Row0 is at the top (keys 1,2,3) and Row3 is at the bottom (keys *, 0, #)
Col0 is on the left (keys 1, 4, 7, *) and Col2 is on the right (keys 3, 6, 9, #)
Pressing a key shorts the corresponding row and column together.

C. J. Kikkert
18 and 19 August 2003