

James Cook University
Electrical and Computer Engineering
EE4306 VHDL Assignment Townsville

Task

Using the MA4A5 Lattice development boards that are used in our labs, design a countdown timer that displays the time left to the end of the event. The timer is to have the following specifications:

- 1 The timer is to use the 2Hz clock on the development boards.
- 2 The maximum time is to be 99 minutes.
- 3 The timer time is to be entered as two variables in the VHDL code. The variables are minutes and seconds. For the code submitted, the time is to be 15 minutes, corresponding to the time available for the Thesis seminars.
- 4 The time remaining is to be displayed on the seven segment display in the form of minutes and seconds remaining. A decimal point is to be used to separate the minutes and seconds.
- 5 Pressing SW1 loads the maximum time and starts the timer process.
- 6 When less than two minutes and more than one minute of time remain, the display will flash at a 1Hz rate. When less than one minute remains the display is to flash at a 4Hz rate.
- 7 The timer is to halt at zero and flash at an 8Hz rate.

Notes:

In practice one might include some jumper settings to set the maximum time. However since 29 of the 32 pins available on the development board are used to drive the seven segment display, not enough pins are available to include this function adequately.

Submission

Submit the complete design before 10am Monday 26 September. The assignment is worth 20 marks being 10% of the total course. Zip the complete directory for the VHDL code and all the resulting ispLever project files and submit this using the safe-assign submission in LearnJCU, by the due date. In addition submit a copy of the VHDL code in electronic form through Safe-assign in LearnJCU. That will then automatically check for any plagiarism.

In addition submit a hardcopy of the user documents, outlining full details of the principles of operation, results of the simulation of the code and including a written copy of the code into the third/fourth year submission slot in the wall or room EL109 by the due date. The hardcopy will be marked for the quality of and the explanations given in the report as well as marks for the code. (The hardcopy will allow me to write comments, for feedback to the student. The electronic files allow me to program the CPLD with your code to verify it's operation.)

To enable me to assess the code, you must specify which compiler (Synplify or Leonardo Spectrum) you have used.

Marking Scheme:

5 marks will be given for documentation outlining the operation of the circuit.

2 marks will be given for the comments contained in the code

6 marks will be given for the VHDL code, it's organisation and function.

3 marks will be given for simulation of the code. (Note the simulation may need to use a slightly modified version of the code to show the resulting waveforms in a reasonable timeframe). No simulation no 3 marks.

4 marks will be given for functionality of the circuit when fitted into the CPLD. To evaluate this I will check that the JED file is produced by your code and I will program it into the CPLD and check the operation of the timer. To get this mark you must have a JED and all the ispLever project files as part of your electronic submission.

Minus 3 marks will given if the Documentation and VHDL code are not clearly labelled with your name and student number.

It is important that each student does this work themselves, to ensure that they learn how to write VHDL code. Safe-assign will automatically check for any plagiarism and will flag to the lecturer any assignments that are similar.

C. J. Kikkert
2 August 2005