

James Cook University
Electrical and Computer Engineering
EE4306 VHDL Assignment Townsville

Task

Using the ispMach M4A5 Lattice development boards that are used in our labs, in conjunction with a 12 bit Digital to Analogue converter, design a basic Direct Digital Synthesis Sinewave generator. The generator is to have the following specifications:

- 1 The clock is to be pin 11 on the IC.
- 2 Pins 42, 41, 40, 39, 38, 37, 36, 26, 25, 24, 27 and 28 on the M4A5 are connected to the 12 Data inputs of the DAC, with pin 42 being the most significant bit and pin 28 being the least significant bit. The M4A5 is to generate the 12 bit values corresponding to the Sinewave output.
- 3 A data clock is to be generated on pin 29, this can be derived from the input clock, to provide a falling edge when the data on the output pins is being changed and a rising edge when valid data is valid to be read by the DAC.
- 4 A Read/Write control line is to be provided on pin 30. This pin is to be low at all times.
- 5 The 12 bit value of the sinewave output is to be determined using a lookup table. The input, representing the phase of the sinewave, is derived from a phase counter. There are to be at least 256 different phase values in that lookup table.
- 5 Those phase values are obtained from a counter, with at least 8 bits.
- 6 Pins 2, 4, 6 and 8 are to be used to control the value at which this phase counter increments. Pin 2 is the most significant bit and pin 8 the least significant bit of a control word. The value of this control word determines the value by which the phase counter is incremented. For example, if the control word is 1000, the counter is incremented by 8. Changing this control word allows the frequency of the generator to be changed.
- 7 Pins 14 and 16 form a 2 bit input to set a phase offset and thus provide a QPSK capability. Pin 14 is the Most-significant bit. The phase offset is to be as follows: Data = 00 phase offset = 0°, Data = 01 phase offset = 90°, Data = 10 phase offset = 180°, Data = 11 phase offset = 270°. This phase offset is added to the phase counter.
- 8 The inputs to pins 2, 4, 6, 8, 14 and 16 are set by jumpers using an external board, connected by a ribbon cable to the development board.

Notes:

You will need to be efficient in the way the Sinewave is generated, and the phase and frequency is controlled, otherwise the code will not fit. We have a DAC board and control board that will be used for testing the submissions.

Submission

Submit the complete design before 10am Monday 11 September 2006. The assignment is worth 20 marks being 10% of the total course. Zip the complete directory for the VHDL code and all the resulting ispLever project files and submit

this using the digital drop-box submission in LearnJCU, by the due date. In addition submit a copy of the VHDL code in electronic form through Safe-assign in LearnJCU. That will then automatically check for any plagiarism.

In addition submit a hardcopy of the user documents, outlining full details of the principles of operation, results of the simulation of the code and including a written copy of the code to A/Prof Kikkert by the due date. The hardcopy will be marked for the quality of and the explanations given in the report as well as marks for the code. (The hardcopy will allow me to write comments, for feedback to the student. The electronic files allow me to program the CPLD with your code to verify it's operation.)

To enable me to assess the code, you must specify which compiler (Synplify or Precision) you have used.

Marking Scheme:

5 marks will be given for documentation outlining the operation of the circuit.

2 marks will be given for the comments contained in the code

6 marks will be given for the VHDL code, it's organisation and function.

3 marks will be given for simulation of the code. (Note the simulation may need to use a slightly modified version of the code to show the resulting waveforms in a reasonable timeframe). No simulation no 3 marks.

4 marks will be given for functionality of the circuit when fitted into the CPLD. To evaluate this I will check that the JED file is produced by your code and I will program it into the CPLD and check the operation of the sinewave generator. To get this mark you must have a JED and all the ispLever project files as part of your electronic submission and those files must contain compiler ticks, indicating that you have properly compiled the code without errors.

Minus 3 marks will given if the Documentation and VHDL code are not clearly labelled with your name and student number.

It is important that each student does this work themselves, to ensure that they learn how to write VHDL code. Safe-assign will automatically check for any plagiarism and will flag to the lecturer any assignments that are similar.

C. J. Kikkert
7 August 2006

VHDL Assignment Marksheet

Name

Student Number

	Max	Award	Comment
Documentation	5		
Comments	2		
VHDL Code	6		
Simulation	3		
Functionality	4		
Penalty	-3		
Total			