

James Cook University
Electrical and Computer Engineering
EE4306 VHDL Assignment 2007

Task

Some dedicated radio transmissions use a simple FFS (Fast Frequency Shifting) modulation, where 4800 the Modulation: FFSK (fast frequency shift keying) modulation, where the data rate and the modulated signal are synchronized and a Logic 1 represented by one half a cycle of 2400Hz and a Logic 0 represented by one full cycle of 4800Hz. The Tone frequencies are phase continuous; transitions of the data occur at the zero crossing point (A modem chip producing this data is CML Microcircuits, CMX469A IC.). The required input and output waveforms are shown in figure 1.

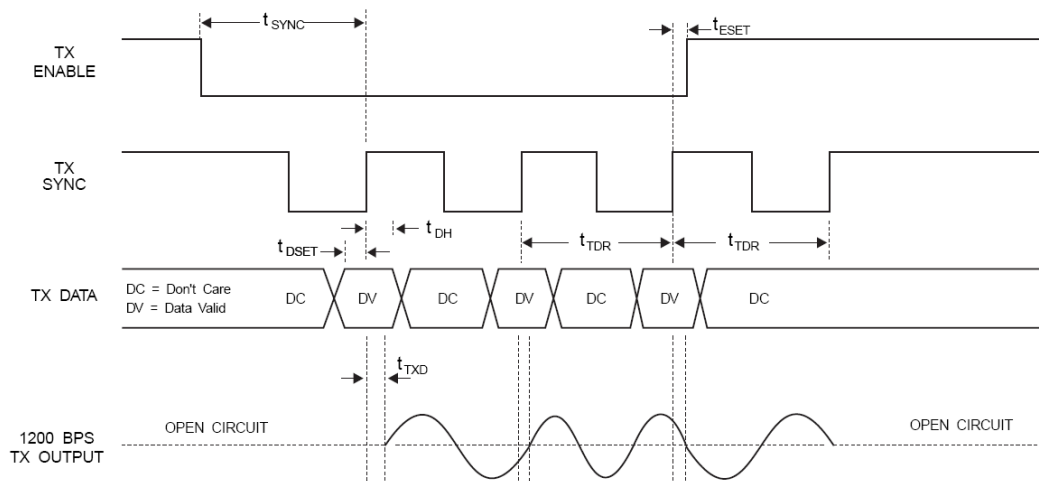


Figure 1. Waveforms for a FFSK transmitter. (from Microcircuits)

The inputs to the FFSK transmitter are a clock of 2 MHz. A TX enable control signal, a serial data input, which is obtained as an RS232 like data stream, using logic level voltages. The TX sync clock and any other clock signals required by your design shown in figure 1 are derived from the 3.6864 MHz clock input. The t_{SYNC} time shown in figure 1, can be as small as needed to ensure that the circuit functions properly. In practice the TX enable signal is generated as a Data_Valid signal by a UART (or equivalent CPLD/FPGA code). The TXdata can be assumed to be synchronised to the TX synch signal, but to allow for timing errors, the TX data must be buffered.

Using the ispMach M4A5 Lattice development boards that are used our labs, in conjunction with an 8 bit DAC like the DAC0800. Write and fully test VHDL code to operate as a FFSK generator. The FFSK generator is to have the following specifications:

- 1 The clock is to be pin 11 on the IC.
- 2 Pins 14, 15, 16, 17, 18, 19, 20 and 21 on the M4A5 are connected to the 8 Data inputs of the DAC, with pin 14 being the most significant bit and pin 21

- being the least significant bit. The M4A5 is to generate the 8 bit values corresponding to the Sinewave output.
- 3 The TX_ENABLE is to be connected to Pins 24, and the TX data is to be connected to Pin 26. (See Note below)
 - 4 The pins will be connected by ribbon cable to boards containing the DAC and data inputs.
 - 5 An AD557 8 bit DAC is used as the DAC. This device includes a data latch and thus requires a clock signal to latch the digital data. The clock for latching the data is to be on pin 8 of the im4a5 and the ribbon cable and is connected to pin 9 (/CE) of the AD557. A Chip select is also required. The chip select is connected to pin 6 of the im4A5 and the ribbon cable and is connected to pin 10 (/CS) of the AD557. The data is latched when the Boolean expression (/CS or /CE) goes Low and the conversion starts then.

Notes:

You will need to be efficient in the way the Sinewave is generated, and the frequency is controlled, otherwise the code will not fit. We have a DAC board and control board that will be used for testing the submissions.

I will use a ispM4A5 development board for generating the TX_Enable and the TX data signals. During the development of the code, I did find a very convenient way of testing the FFSK modulation was by generating suitable TX_enable and TX data signals inside the same CPLD that produces the FFSK. (These is enough spare capacity to allow for this.) It is permissible to use this option for your final submission. Please specify in your submission document and the VHDL code, which option you use, to permit me to accurately test your submission.

Submission

Submit the complete design before 10am Monday 10 September 2007. The assignment is worth 20 marks being 10% of the total course. Zip the complete directory for the VHDL code and all the resulting ispLever project files and submit this using the digital drop-box submission in LearnJCU, by the due date. In addition submit a copy of the VHDL code in electronic form through Safe-assign in LearnJCU. That will then automatically check for any plagiarism.

In addition submit a hardcopy of the user documents, outlining full details of the principles of operation, results of the simulation of the code, including a written copy of the code and with the attached mark sheet with your name included as the front page, to A/Prof Kikkert by the due date. The hardcopy will be marked for the quality of and the explanations given in the report as well as marks for the code. (The hardcopy will allow me to write comments, for feedback to the student. The electronic files allow me to program the CPLD with your code to verify it's operation.)

To enable me to assess the code, you must specify which compiler (Synplify or Precision) you have used.

Marking Scheme:

5 marks will be given for documentation outlining the operation of the circuit.

1 mark will be given for the comments contained in the code

7 marks will be given for the VHDL code, its organisation and function.

3 marks will be given for simulation of the code. (Note the simulation may need to use a slightly modified version of the code to show the resulting waveforms in a reasonable timeframe). No simulation no 3 marks.

4 marks will be given for functionality of the circuit when fitted into the CPLD. To evaluate this I will check that the JED file is produced by your code and I will program it into the CPLD and check the operation of the sinewave generator. To get this mark you must have a JED and all the ispLever project files as part of your electronic submission and those files must contain compiler ticks, indicating that you have properly compiled the code without errors. Ensure that your submission contains your JED file. No JED file no 4 marks.

Minus 3 marks will given if the Documentation and VHDL code are not clearly labelled with your name and student number. Also please ensure that your submission can easily be identified. Do not submit the file as Assignment.Zip, rather use YourName.zip. This ensures that no submissions are overwritten during the downloading.

It is important that each student does this work themselves, to ensure that they learn how to write VHDL code. Safe-assign will automatically check for any plagiarism and will flag to the lecturer any assignments that are similar.

C. J. Kikkert

V1 -7 August

V3 -28 August 2007

VHDL Assignment Marksheet

Name

Student Number

	Max	Award	Comment
Documentation	5		
Comments	1		
VHDL Code	7		
Simulation	3		
Functionality	4		
Penalty	-3		
Total			