

**James Cook University**  
**Electrical and Computer Engineering**  
**EE4306 RF Design Assignment**

***Aim***

The aim of this assignment is to firstly provide some experience in the design and optimisation of RF circuits. This assignment is worth 20% of the total mark for the subject.

***Requirements:***

Design a low noise amplifier using the Avago's ATF-35143 high dynamic range, low noise, PHEMT, which is housed in a 4-lead SC-70 (SOT-343) surface mount plastic package. The input and output are to be compatible with either a 50  $\Omega$  or a 75  $\Omega$  characteristic impedance system, depending on the specifications set for you. The input VSWR should be less than 2:1 for the allocated frequency range. A supply voltage of up to 5V is available. The low noise amplifier can be mounted on a FR4 PCB material. For FR4, the board has a thickness of 1.52 mm thickness and is copper plated with a 1 oz copper cladding (0.035mm thick). FR4 has a dielectric constant of approximately 4.7 and a loss tangent of 0.014. FR4 does not have well controlled RF properties.

Your design should include noise figure and output power (such as 1dB compression) determinations for your amplifier. Your design should be unconditionally stable and have as low a noise as possible. The bandwidth of the amplifier should be at least the bandwidth specified specifically for you.

The design to be produced by each student should include a full PCB layout and its corresponding Gerber plot file. PCB mounting SMA connectors are to be used for the connectors to get the signals on and off the board. These connectors can be in any suitable configuration, but they must be able to provide a good RF connection and be soldered directly to the board. The circuit is to occupy the smallest possible printed circuit board area.

Each student has to write a report providing full design, layout and optimisation details of the design. The circuit schematic design must be verified using computer simulation. A paper copy of the design report is to be submitted by **10 am Monday 3 November 2008** to A/Prof Kikkert. The Microwave Office and Gerber Plot files are to be Zipped and the Zip file should be submitted using digital drop box in LearnJCU by the same deadline. The report (doc or txt) file is to be submitted using Safe-assign in LearnJCU. The MWO files must have your name and student number as text in the Schematic file. **Safe-assign will detect plagiarism.**

Each student is given a different minimum RF bandwidth and impedance to design for, according to the following table:

Surname	Given Name	Frequency	Impedance
Anderson	Liam James	800-1200	50
Authurs	Wade Jared	900-1300	50
Bajema	Casey William	1000-1400	50
Bajema	Grant Jacob	1100-1500	50
Brennan	Craig Michael	1200-1600	50
Carter	Christopher	1300-1700	50
Daltonalomes	Scott	1400-1800	50
Davis	Owen Stephen	1500-1900	50
De Jager	Jean-Pierre	850-1250	75
Evans	Adrian James	950-1350	75
McNicol	James Douglas Tang	1050-1450	75
Meerkotter	Monique	1150-1550	75
Nash	Matthew Richard	1250-1650	75
Olsen	Natalie Susan	1350-1750	75
Payet	Selwyn Allen	1450-1850	75
Rees	Matthew Bernard	1550-1950	75
Xie	Rong	1150-1550	50

The marking scheme is on the next page and that page must be attached to your assignment, to permit the appropriate feedback.

C. J. Kikkert

15 Sep 2008, V2 update 22 Oct 2008

## **RF Assignment Marking Scheme**

6 marks will be given for documentation outlining the operation of the circuit.

Your documentation should include all the circuit diagrams, and screen shots of the performance of the circuit.

8 marks will be given for the RF design i.e. the performance of the amplifier.

These marks will include the following performance indicators:

- 1 How well does the circuit work as an amplifier ?
- 2 What is the noise figure, 1 dB compression point and output power
- 3 How costly is it to manufacture ( size, tolerances required etc) ?
- 4 Are the bandwidth requirements satisfied ?

5 marks will be given for the circuit layout.

Factors to be considered here are the overall size of the circuit, the real estate utilisation, the avoidance of unwanted coupling and the shielding provided by the ground-plane.

1 mark will be given for the Gerber plot files.

**Minus 3 marks will given if the Documentation and Gerber Plot files are not clearly labelled with your name and student number.**

**Name:**

	Max	Mark	Comment
Documentation	6		
RF design	8		
Layout	5		
Plot files	1		
Name in Docs	-3		
Total			

## Solution

### Introduction

Any design like this requires firstly the assembly of data about the device to be used. Since the device is made by Avago, the selection guides from Avago, show their product range and included the ATF-35143 device. [http://www.avagotech.com/pages/en/rf\\_ics\\_discretes/transistors/gaas\\_field\\_effect/](http://www.avagotech.com/pages/en/rf_ics_discretes/transistors/gaas_field_effect/)

Selecting the ATF-35143 device web page allows the data sheet and some application notes to be obtained. Avago's application note 1174 shows a suggested Schematic diagram for biasing the FET. It is a good idea to carefully read the manufacturer's application notes 1174 and 1271 on this device as well as the data sheet prior to attempting a design.

The data sheet provides biasing data, s-parameter data and parameters for the STATZ MESFET model to permit a non-linear analysis to be carried out if needed. The data sheet however indicates that the s-parameter data should be used for better accuracy.

For this design, a centre frequency of 1.2GHz is used and the aim of the design is an amplifier suitable for 700MHz to 1.7GHz, covering the entire output frequency band of a typical Low Noise Block-converter LNB used in satellite reception.

For this solution a  $V_{ds}$  of 3 Volt is used and an  $I_{ds}$  quiescent current of 15 mA is also used. Figure 1 of the data sheet then indicates that a  $V_{gs}$  voltage of 0.6 Volt is required. Resistors R2 are the self biasing resistors. For 15mA and 0.6V, the total resistance is  $40\Omega$ , so that two  $82\Omega$  resistors are required for R2. Application note 1174 suggests two  $47\Omega$  resistors for a quiescent current of 10mA for a  $V_{ds}$  of 2Volt. Figure 1 suggests a  $V_{gs}$  of 0.5V for this, resulting in a  $100\Omega$  resistor. This is higher than the value suggested in application note 1174 and some experimentation may be required once the circuit is built. The value of R2 does not effect the RF circuit since R2 is bypassed by C3 and C4 in figure 2 of AN1174 at all RF frequencies. This information is used to draw the schematic for the basic amplifier as shown in figure 1.

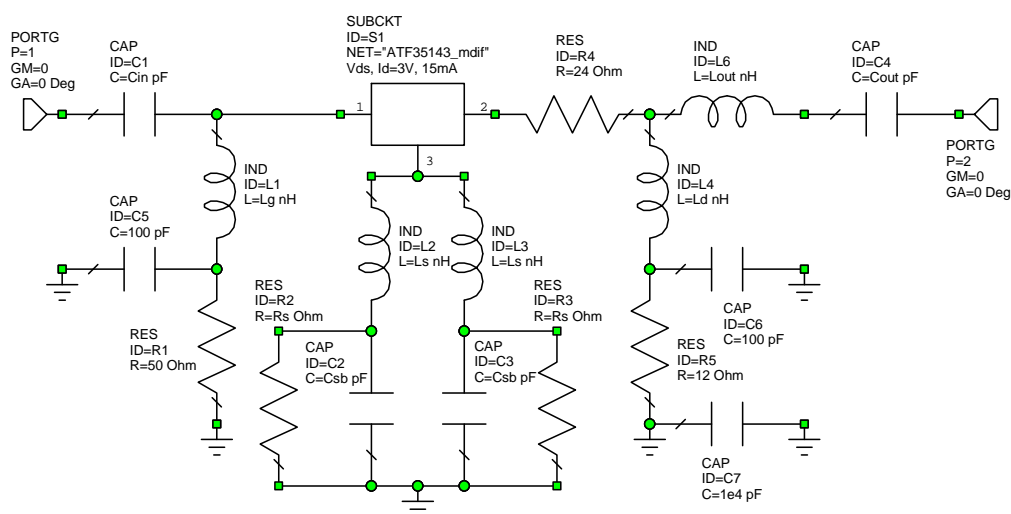


Figure 1. Basic Low Noise Amplifier.

PortG ports which give a device match rather than the normal  $50\Omega$  Ports are used. The first step is to determine the input and output impedances of the circuit. Resistor R1 provides stability at low frequencies and resistor R4 is needed to provide unconditional stability at the operating frequency. The values used initially are those suggested in AN1174. The input and output coupling capacitors C1 and C4 are  $100\text{ pF}$  and close enough to a short circuit at  $1.2\text{ GHz}$ . The RFC L1 and L4 are  $470\text{ nH}$  and are close enough to an open circuit at  $1.2\text{ GHz}$ . The resulting input and output impedances are shown in figure 2.

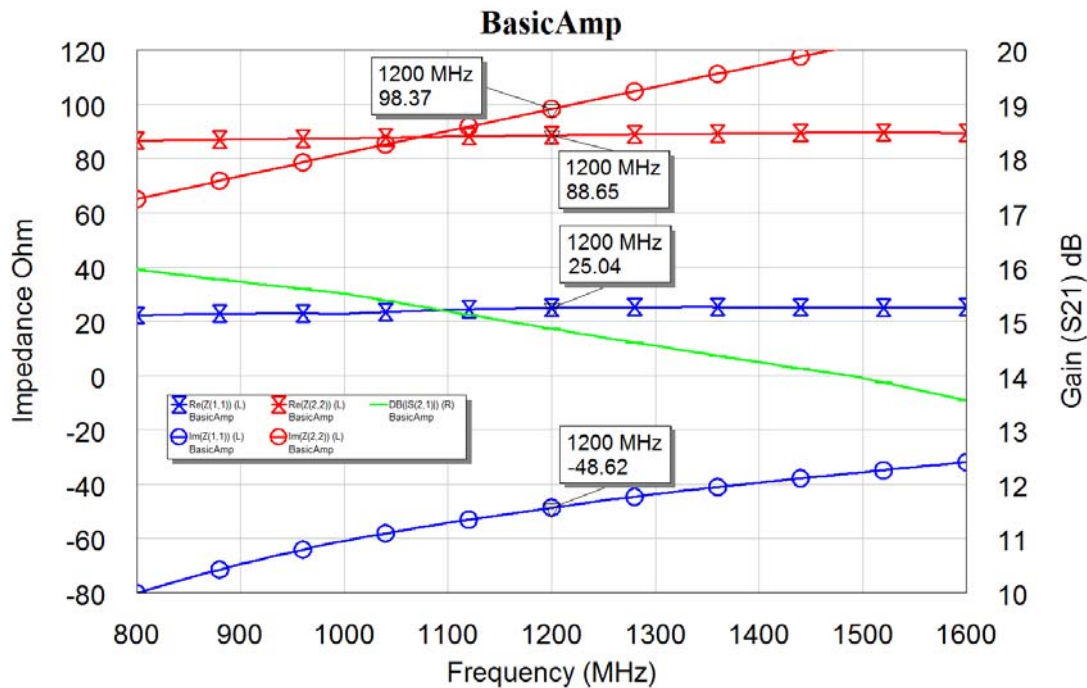


Figure 2. Input and output impedances for the Basic Low Noise Amplifier.

The input impedance is thus  $25 - j48.6\ \Omega$  and the output impedance is  $88.7 + j98.4\ \Omega$ . Matching networks need to be designed for this. Since a broadband design is required, multistage matching networks are required. To design those, the input impedance as a parallel network is required. Applying series to parallel conversion equations or using MWO to calculate the conversions, by measuring the input impedance of a resistor in parallel with a capacitor and matching the resulting input impedance with figure 2, gives the input as a  $120\ \Omega$  resistor in parallel with a  $2.15\text{ pF}$  capacitor. Similarly the output corresponds to a  $178.3\ \Omega$  resistor in parallel with a  $-0.67\text{ pF}$  capacitor. A negative capacitor is physically not possible, but simply means that we need to increase the capacitance by  $0.67\text{ pF}$  in out matching circuit.

Figure 3 shows the resulting single stage matching network for the input. The  $2.15\text{ pF}$  capacitor corresponds to the input capacitance. The network Q is adjusted till the matching capacitance required is the same as the input capacitance. Figure 4 shows the output matching network for the same Q value as the input.

These values are now entered into the schematic for the amplifier. The capacitance at the device end of the output matching network is  $1.562 + 0.67 = 2.232\text{ pF}$ . The circuit is simulated and the capacitances are tuned slightly to provide a better match, with the resulting circuit shown in figure 5 and the corresponding performance in figure 6.

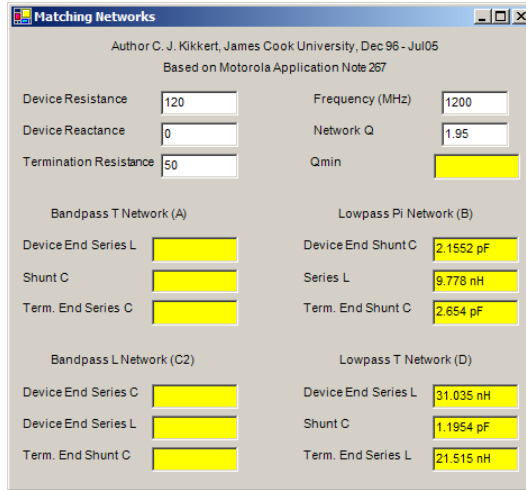


Figure 3. Input matching network.

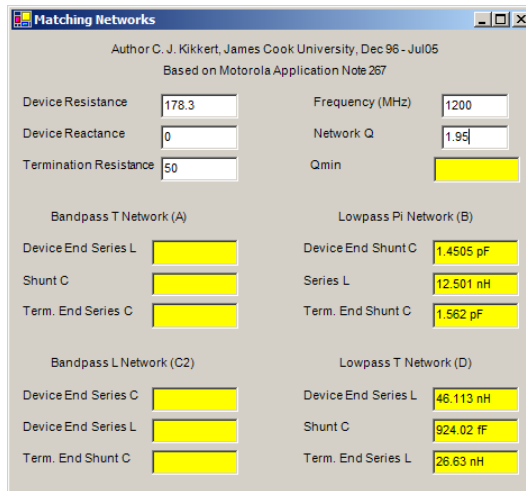


Figure 4. Output matching network.

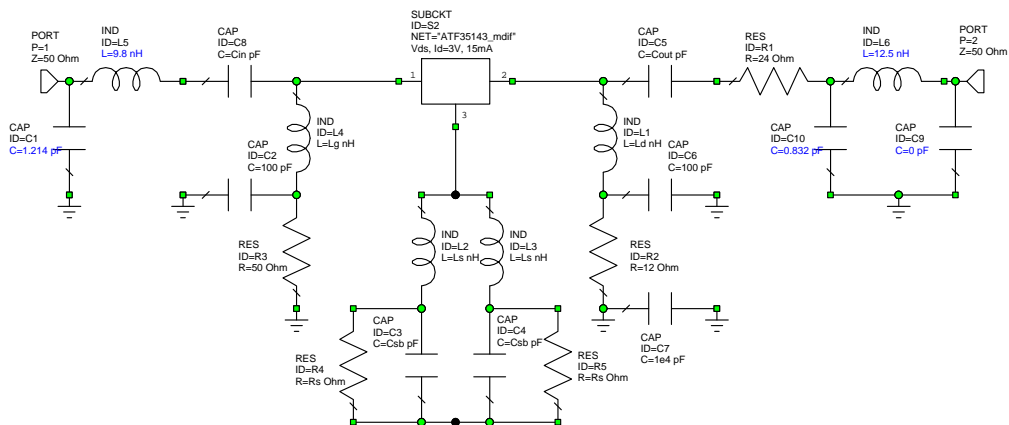


Figure 5. Low noise amplifier with matching networks.

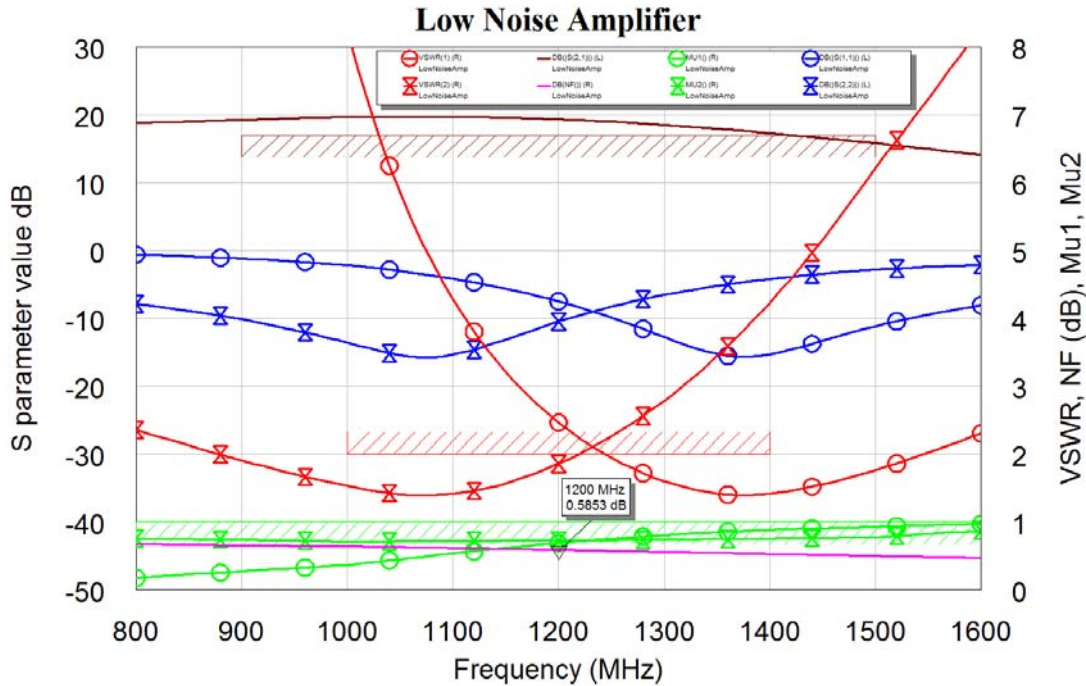


Figure 6. Performance of amplifier of figure 5.

Often one only uses  $S_{11}$  and  $S_{22}$  to observe the input and output reflection coefficients. In this design a VSWR limit is specified, so that is plotted and the optimisation limits are set using the VSWR, as indicated by the red curves in figure 6. The noise figure of the amplifier is 0.58 dB.

The initial design using the impedance calculated matching elements gives a sufficiently close performance, that the optimum performance can be achieved using the optimisation tools or fine tuning tools available in MWO. During the fine tuning it is obvious that there is a large interaction between the input and output networks. Tuning the output also changes the input S parameters. This is expected since  $S_{12}$ , the return gain is significant, as it is with most RF transistors.

A major problem is the stability, since the input and output stability factors  $Mu1$  and  $Mu2$  are both less than 1, indicating conditional stability. Increasing the  $24 \Omega$  series resistor, increases the stability and changes  $S_{11}$  and  $S_{22}$  and NF as well.

Optimising the matching networks using the random local optimiser, results in the component values shown in figure 7 and the performance shown in figure 8. The stability has been increased by increasing  $R6$  to  $156 \Omega$ . To investigate the effect of that resistor on the noise figure, a resistor model (REST) which includes the thermal noise of that resistor is used. The noise contribution due to that resistor is 0.002 dB and can thus be neglected. Since the performance specifications cannot be met, a broader band matching network needs to be used, or the specifications must be relaxed.

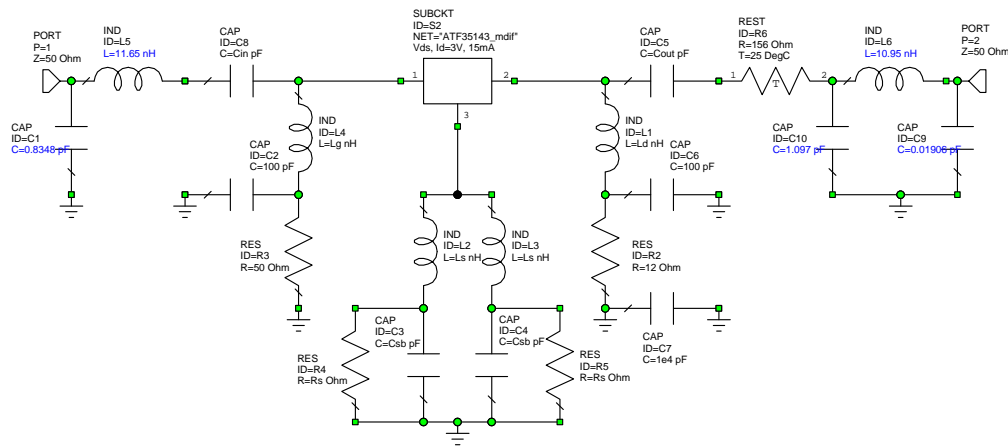


Figure 7. Circuit of figure 5 after optimisation.

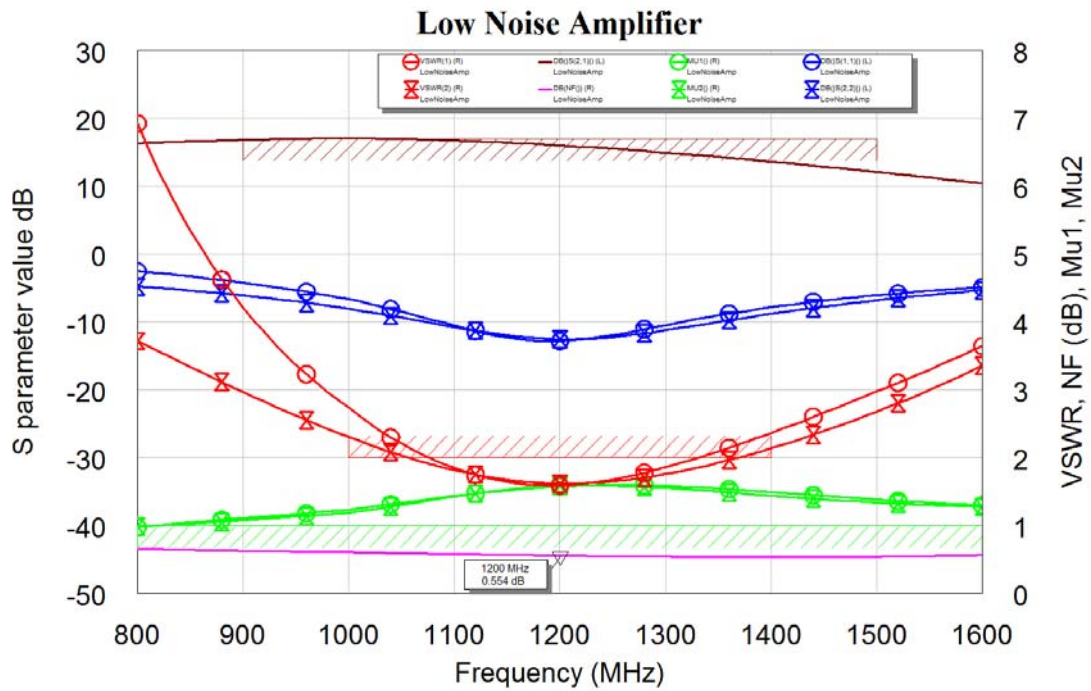


Figure 8. Performance of amplifier of figure 7.

Broadband matching using a 3 stage input matching network is applied to the input and since the impedance transformation required for the output is less, a 2 stage matching network is used for the output. For the input, the termination impedances of the stages will be 120  $\Omega$ , 90  $\Omega$ , 66  $\Omega$  and 50  $\Omega$  for nearly equal impedance transformation ratios. A network Q of 1.9 is used for the matching networks.

For the output network, since the Q of the device output is smaller, a lower Q network can be used and a two stage impedance transformation should be able to be used. Resulting in a 178  $\Omega$ , 94  $\Omega$  and 50  $\Omega$  terminating impedances of the matching stages. To obtain reasonable component values a network Q of 1.5 is used. The matching components of the circuit and the series resistor, all shown in blue in figure 9 are then optimised, resulting circuit shown in figure 9, with the corresponding performance shown in figure 10. The circuit is now stable and is close enough to just meet the

specifications. However the noise figure has increased significantly and is high for what is expected to be a low noise amplifier.

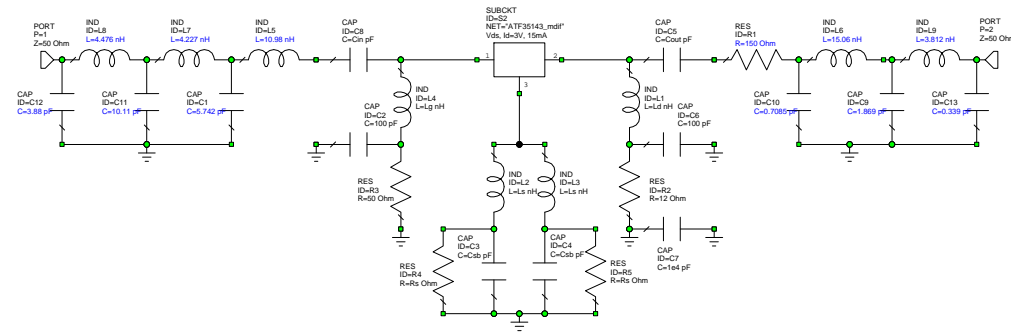


Figure 9 Low Noise Amplifier with broadband matching.

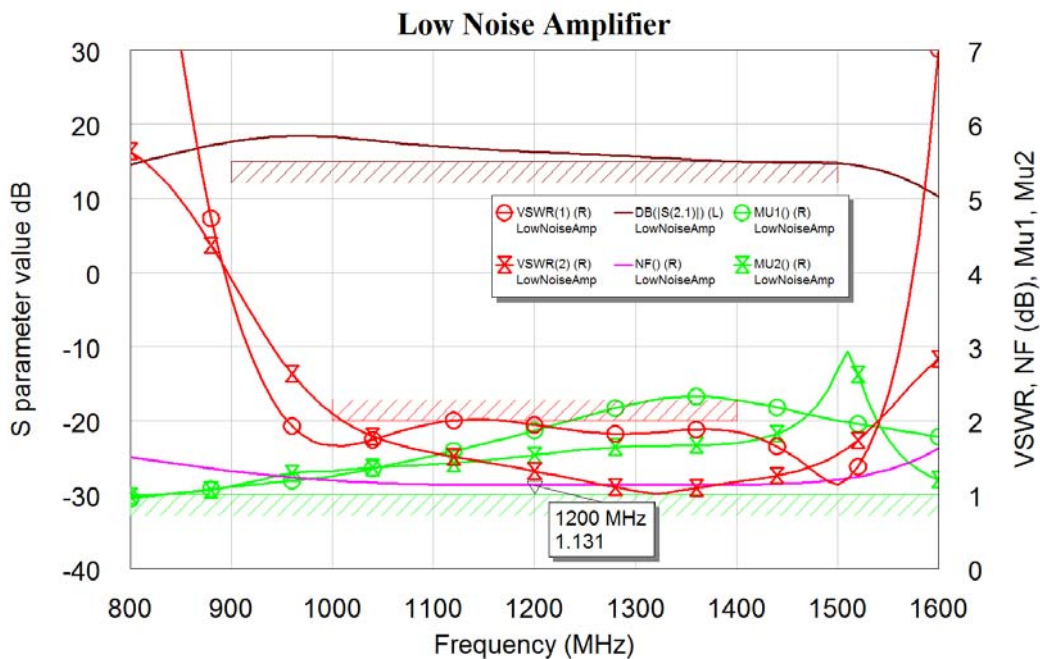


Figure 10. Performance of amplifier of figure 9.

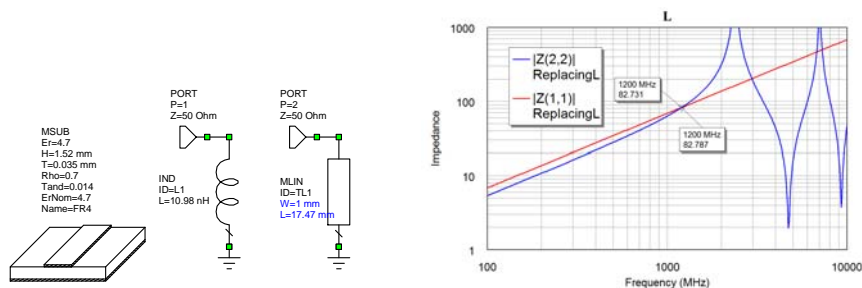


Figure 11. Replacing Inductors with transmission lines.

Since the inductors are very small, they need to be replaced by transmission lines. The width and length of the transmission line used is chosen to firstly ensure that the circuit can be easily made and does not have to high a loss, as a result the minimum width of the transmission line is chosen to be 0.5 mm. Secondly the length of the

transmission line is adjusted to result in the same inductance. This is easily done using MWO as shown in figure 11.

Once the inductors of the matching networks have been replaced with transmission lines, the circuit is further optimised, resulting in the circuit of figure 12, with the corresponding performance shown in figure 13. The amplifier now meets the VSWR specification easily but the noise figure is still relatively high.

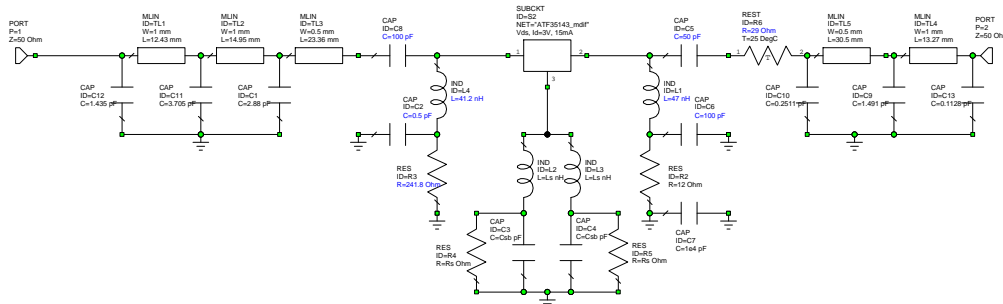


Figure 12. Circuit of figure 9, with inductors replaced by transmission lines after optimisation.

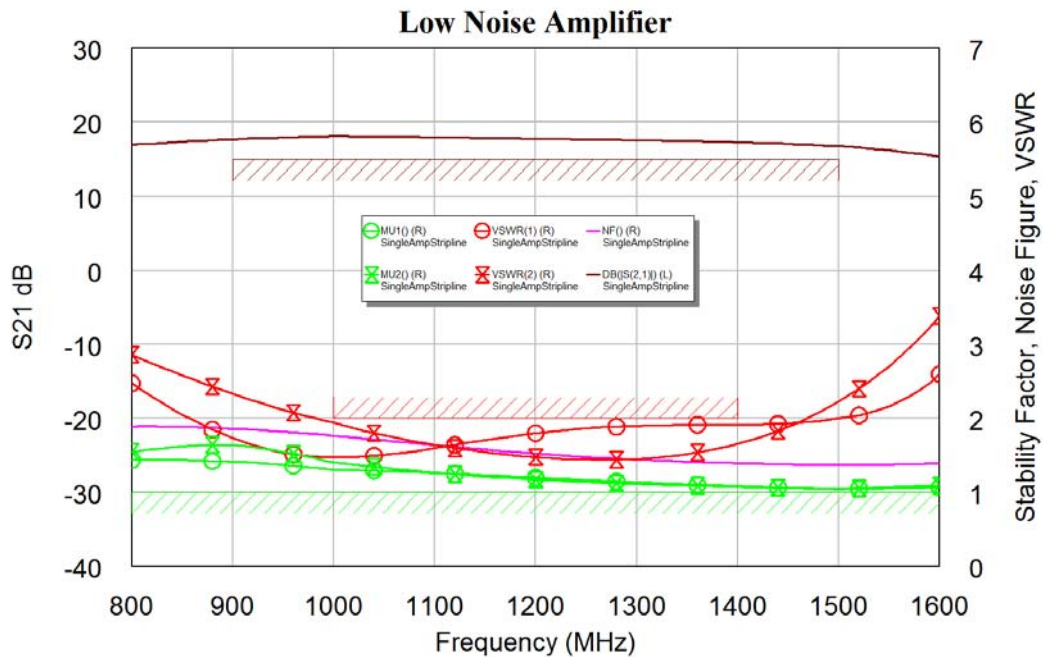


Figure 13. Performance of the amplifier of figure 12.

The decision then has to be made to:

- 1) Accept the performance, including the noise performance for the circuit of figure 7.
- 2) Try a different approach and ensure that the noise figure remains well below 1. One approach is to use transmission lines for the impedance match. The length and impedance of a transmission line required for the impedance transformation can easily be calculated. Applying that however still gives a narrow-band match and cannot meet the specifications. A two stage amplifier outlined below is another approach.

## Two stage amplifier

It is possible to use one FET to drive another. That will firstly reduce the reverse gain, thus reducing the interaction between the input and output impedances. Secondly, it will increase the gain from the amplifier, to ensure that the output signal is sufficiently above the noise, that the noise figure of any complete system is not effected by the succeeding circuits. The basic amplifier now has the circuit shown in figure 14.

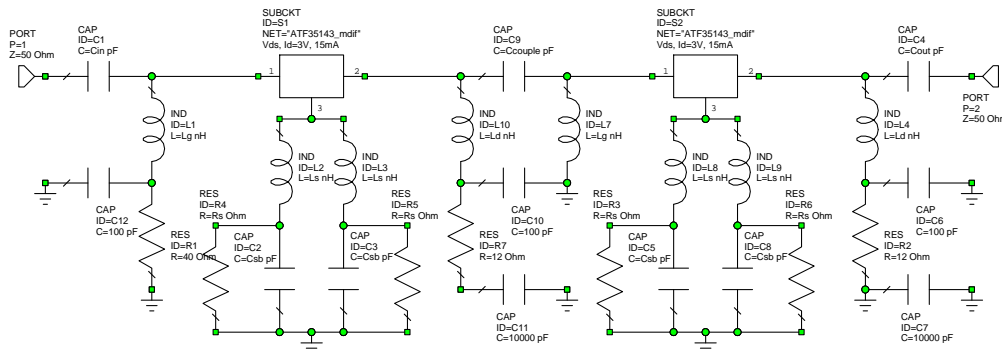


Figure 14. Basic Low Noise Amplifier Circuit with 2 FET's.

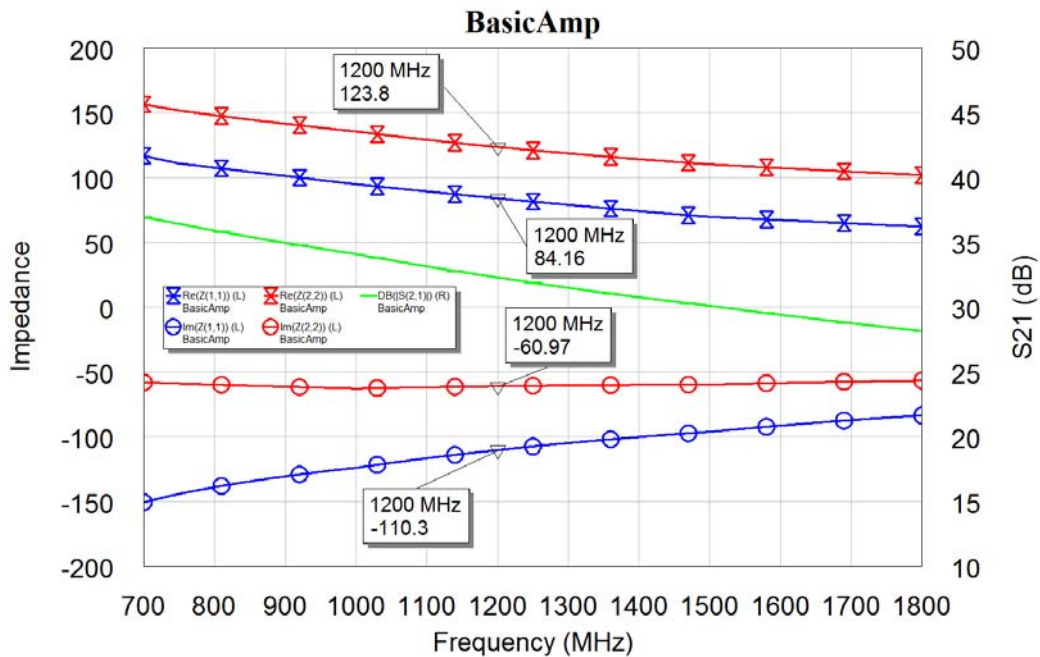


Figure 15. Impedances of the amplifier of figure 14.

The impedance matching as described above is then performed. Firstly, the series input impedance of  $84.16 - j110.3 \Omega$  is transformed to a parallel RC network, resulting in a  $230 \Omega$  resistor in parallel with a  $0.76\text{pF}$  capacitor for the input. Then two pi section matching networks are used with the centre impedance of  $107 \Omega$ , being the geometric mean of the  $230 \Omega$  input resistance and the required  $50 \Omega$  terminating impedance. The same process is done for the output impedance. The impedance of  $123.6 - j60.97 \Omega$  corresponds to a  $154 \Omega$  resistance in parallel with a  $0.425\text{pF}$

capacitance. The resulting two pi section matching networks have a centre impedance of  $87.7 \Omega$ , being the geometric mean of the  $154 \Omega$  output resistance and the required  $50 \Omega$  terminating impedance. Optimising the matching network elements results in the circuit shown in figure 16.

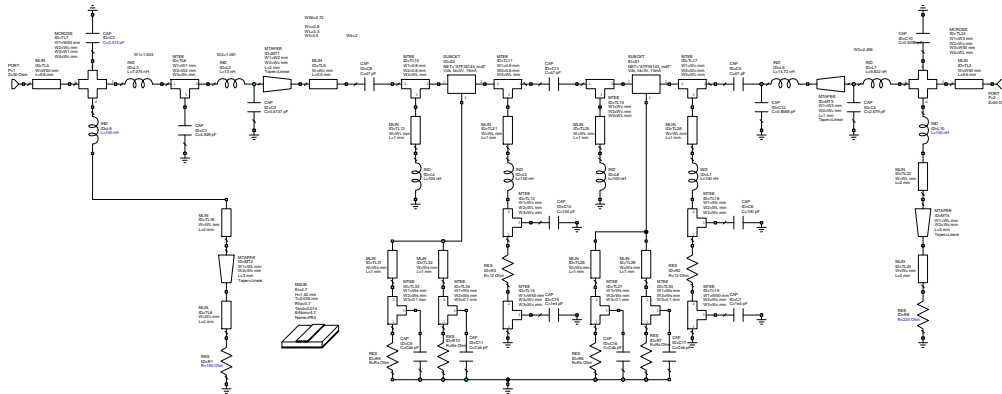


Figure 16. Optimised Broadband LC Matching for Low Noise Amplifier Circuit with 2 FET's.

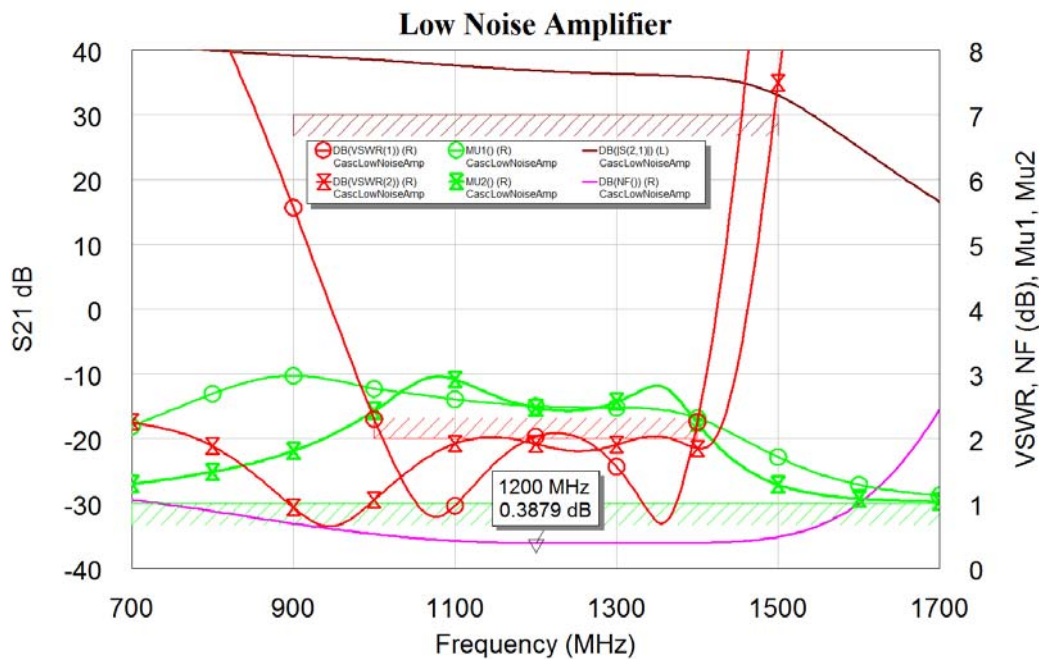


Figure 17. Performance of the amplifier of figure 16.

Since the inductors are too small to be realised reliably, the inductors are replaced with microstrip lines. Further optimisation is carried out and if needed changes are made to ensure that the amplifier is stable at all frequencies. This results in the following circuit shown in figure 18. In order to minimise the number of inductors used, the input stability resistor is connected to the inductor at the gate of the first FET. This does increase the noise figure by about 0.05 dB. The losses in the microstrip lines, compared to the ideal inductors used for the circuit of figure 16, also increase the noise figure, but as can be seen from figure 19, the resulting noise figure of 0.64 dB at 1200 MHz is still very good. Figure 20 shows that the amplifier is stable at all frequencies. Figure 21 shows the resulting PCB layout.

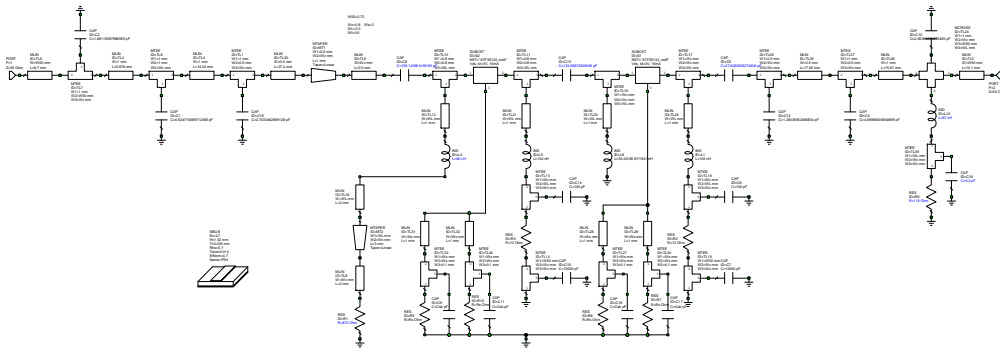


Figure 18. Final Low Noise Amplifier Circuit with 2 FET's.

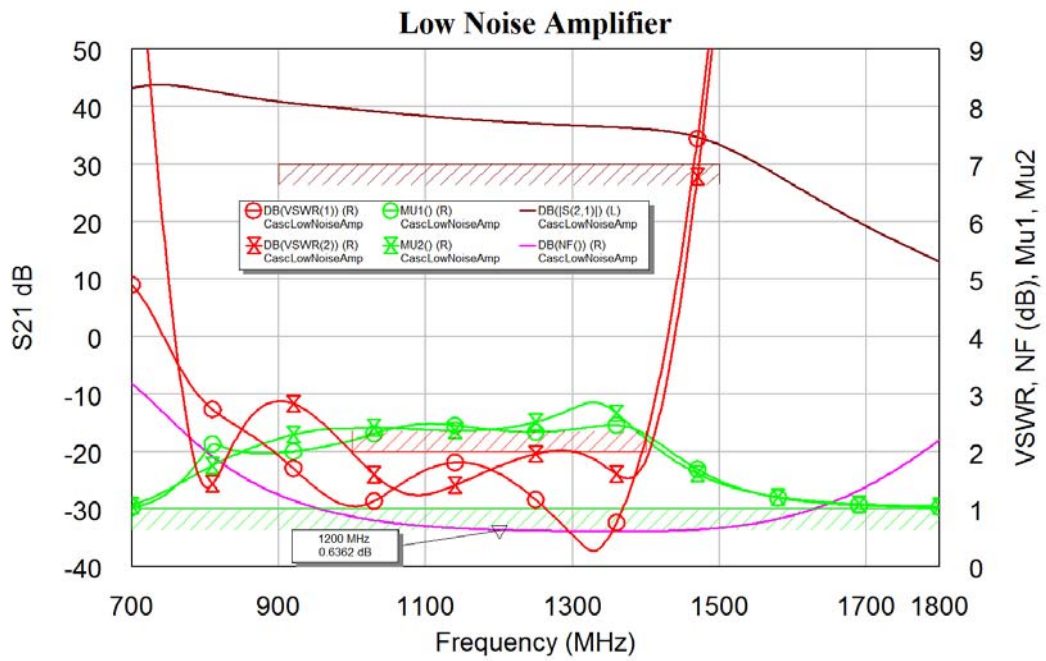


Figure 20. Performance of the amplifier of figure 19.

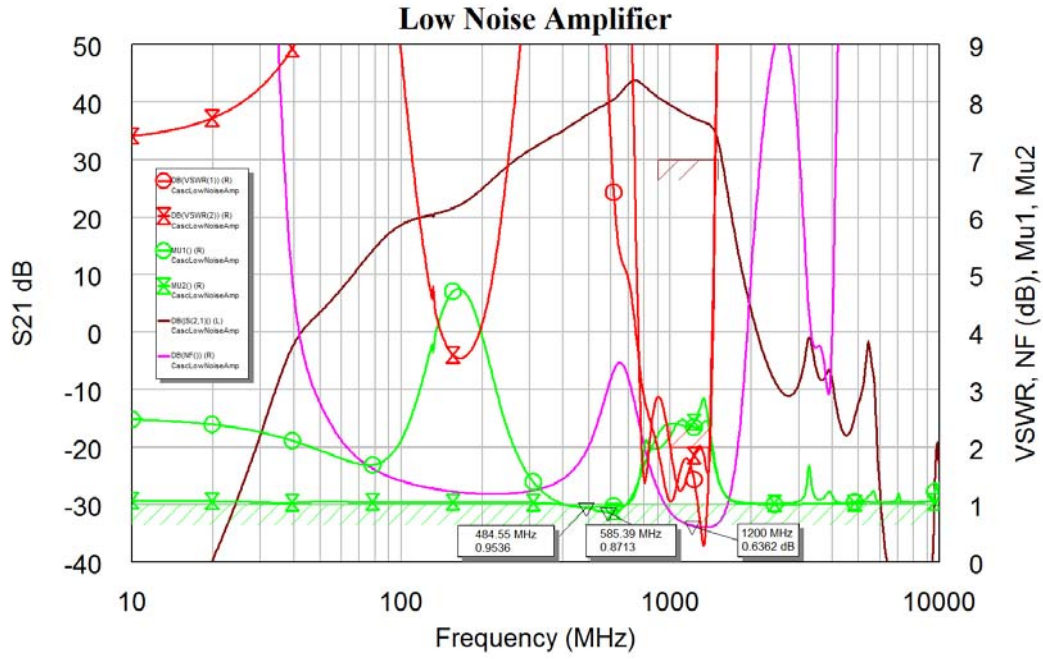


Figure 21. Stability check of the amplifier of figure 19.

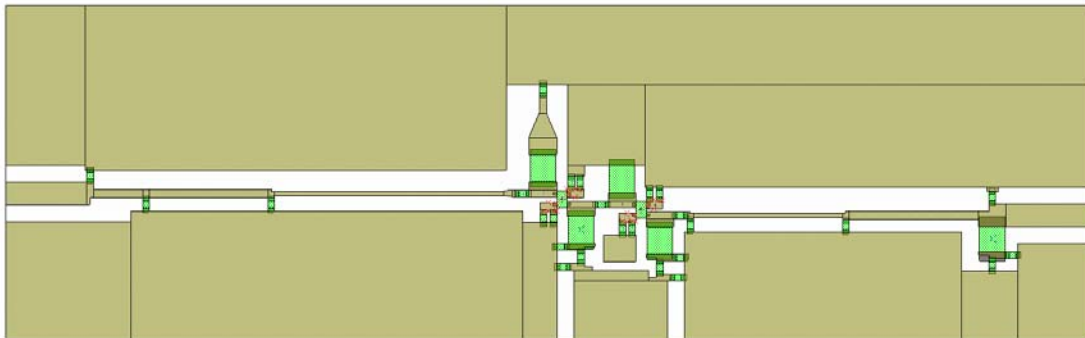


Figure 22. Final PCB layout of the amplifier of figure 19.