James Cook University
Electrical and Computer Engineering
EE4306 VHDL Assignment 2008

Task

Design hardware to convert a fixed point integer into a floating point integer number. The input is a 16 bit integer, connected to pins 2 to 9 and 14 to 21 of the Lattice IC used in the ispM4A5 development boards, with pin 2 corresponding to the most significant bit and pin 21 being the least significant bit. The output is to have an 8 bit mantissa and a 4 bit exponent. As an example the 16 bit integer X"A346" is to be converted to the binary number 10100011 x 2^7, where "10100011" = X"A3" is the mantissa, being the most significant part of the integer and 8 corresponding to 2^8 is the exponent. Similarly X"0046" would result in a mantissa of X"46" and an exponent of X"0". Further examples are shown in the table below:

Integer	Mantissa	Exponent
X"A346"	X"A3"= 1010 0011	8
X"5346"	X"46"= 0100 0110	7
X"0346"	X"34"= 0011 0100	4
X"0046"	X"46"= 0100 0110	0
X"0006"	X"06"= 0000 0110	0

The exponent is to be connected to pins 43 to 40, with 43 being the most significant pin. The 4 most significant bits of the mantissa are to be connected to pins 39 to 36, with pin 39 being the most significant digit. The 4 least significant bits of the mantissa are to be displayed as a Hexadecimal number using the seven segment display connected to pins 31 to 24 of the IC.

Testing:

The main testing should be done using waveforms. You may consider using Matlab, C or other ways to generate test vectors for all the possible 65536 input combinations and using the same software to generate the desired output. That will ensure that your circuit operates perfectly.

In addition you will need to test the hardware realisation. The input signals can be generated in two ways. Firstly one can use a test board with jumpers to set the input pins to the required level. Secondly another ispM4A5 development board can be used to operate a counter and generate all the input signals. (A VHDL program is required to do this.) This test board is then connected to the board with the code for the assignment using a ribbon cable. The ribbon cable must be twisted to ensure that Vcc and Gnd line up on both ends of the cable. Failure to do this will result in damage to the boards. Also ensure that the clock on the board with the integer to floating point converter is disabled by not having any jumpers connecting the clock. (Park the jumper on one pin only to prevent its loss.) The output can be tested in a similar way and the assignments will be marked using this technique. Since we only have a limited number of ispM4A5 development boards, students will need to share boards. Make sure that you complete the assignment early, so that you will be able to access sufficient boards to fully test your realisation.

Submission

Submit the complete design before 10am Monday 6 October 2008. The assignment is worth 20 marks being 10% of the total course. Zip the complete directory for the VHDL code and all the resulting ispLever project files and submit this using the digital drop-box submission in LearnJCU, by the due date. In addition submit a copy of the VHDL code in electronic form through Safe-assign in LearnJCU. That will then automatically check for any plagiarism.

In addition submit a hardcopy of the user documents, outlining full details of the principles of operation, results of the simulation of the code, including a written copy of the code and with the attached mark sheet with your name included as the front page, to A/Prof Kikkert by the due date. The hardcopy will be marked for the quality of and the explanations given in the report as well as marks for the code. (The hardcopy will allow me to write comments, for feedback to the student. The electronic files allow me to program the CPLD with your code to verify it's operation.)

To enable me to assess the code, you must specify which compiler (Synplify or Precision) you have used.

Marking Scheme:

5 marks will be given for documentation outlining the operation of the circuit.

1 mark will be given for the comments contained in the code

7 marks will be given for the VHDL code, it's organisation and function.

3 marks will be given for simulation of the code. (Note you are encouraged to test your code using all the 65536 input combinations. However your submission should have less than 1024 test vectors, to ensure that the assignment can be marked in a reasonable time.). No simulation or more than 1024 test vectors, no 3 marks.

4 marks will be given for functionality of the circuit when fitted into the CPLD. To evaluate this I will check that the JED file is produced by your code and I will program it into the CPLD and check the operation of the sinewave generator. To get this mark you must have a JED and all the ispLever project files as part of your electronic submission and those files must contain compiler ticks, indicating that you have properly compiled the code without errors. Ensure that your submission contains your JED file. No JED file no 4 marks.

Minus 3 marks will given if the Documentation and VHDL code are not clearly labelled with your name and student number. Also please ensure that your submission can easily be identified. Do not submit the file as Assignment. Zip, rather use YourName.zip. This ensures that no submissions are overwritten during the downloading. Ensure that the zipped directory containing your code is named appropriately to be able to identify you, do not name the directory assignment, as I will then end up with 30 directories called assignment during marking, making it very difficult to correctly identify your work.

It is important that each student does this work themselves, to ensure that they learn how to write VHDL code. Safe-assign will automatically check for any plagiarism and will flag to the lecturer any assignments that are similar.

C. J. Kikkert

8 August 2008, V2 26 Aug.

VHDL Assignment Marksheet

Name

Student Number

	Max	Award	Comment
Documentation	5		
Comments	1		
VHDL Code	7		
Simulation	3		
Functionality	4		
Penalty	-3		
Total			