

# James Cook University

## Electrical and Computer Engineering

### E4301 VHDL Programming

#### **Aim**

The aim of the experiment is to provide students with some experience in writing and debugging VHDL code.

#### **Procedure**

Use the Synplify or Precision software to write the code for a Hexadecimal (4 bit) counter to drive the right display of the development Lattice board. The counter is to run normally and is to halt when switch SW1 is pressed (i.e. when pin 7 on the device is low)

Verify the counter waveforms using either the VHDL or ABEL waveform viewers.

Program the M4A4 IC on the Lattice Board and verify the operation of the counter.

#### **Programming hints**

To start a VHDL program in the ispLever Project Navigator use **Source** ⇒ **New** and select VHDL from the dialog box.

Some VHDL projects and their source code examples are located on the EE4306 web under Resources/Examples.

The circuit diagram and the pin connections for the Development board are on the Lattice CD and a step by step tutorial for starting a project using Synplify is in the “LatticeHDLSynplifytutor2.pdf” in the VHDL-Language directory of the Lattice CD. That file is also linked to the EE4306 laboratory web page, where this file is kept.  
<http://eng.jcu.edu.au/subjects/ee4306/practicals/index.shtml>.

In addition a good resource is the Precision RTL\_style.pdf document (322 pages) on the Lattice CD under Manuals/precision/

Techniques for pin locking are described in the lecture notes.

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