

EE4306 Tutorial 2

VHDL Programming

Task:

An up/down counter is required. The counter has a Clock and Reset input and the count value and up/down indicator as outputs. When the Reset is low, the counter is set to zero. When Reset is high, the counter counts up to 31, it remains at 31 for one clockpulse and counts down to zero, when it gets to zero, it remains at zero for one clockpulse and then counts up again. When it gets to 31, the process is repeated.

- 1 Write the complete code using integers for the counter.
- 2 Write the code using standard logic vectors for the counter.

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