

EE4306 Tutorial 3

VHDL Programming

Task:

Write VHDL modules for an adder which adds two 8 bit wide signals, A and B and produces a 8 bit wide sum and a carry output is possible. The problem is to be solved three ways:

- 1 Using a loop as shown on page 20 of the EE4306 VHDL language lecture notes.
- 2 Using components as shown on pages 24 of the EE4306 VHDL language lecture notes.
- 3 Using arithmetic as shown on page 13 of the EE4306 VHDL language lecture notes.

Using the ispMach4A5 CPLD, compare the number of Logic Product Terms and MacroCells used for each realisation.

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