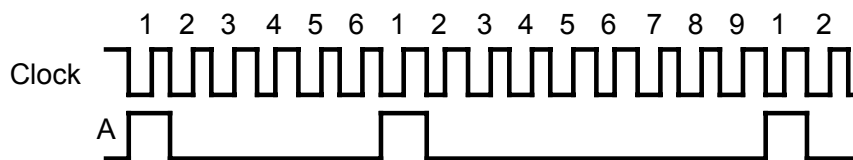


# EE4306

## VHDL Tutorial Problems

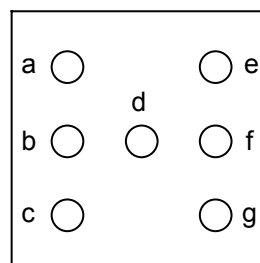
### Problems

- 1 Write the VHDL Code for a circuit to generate the sequence:  
1, 2, 3, 5, 8, 13, 21, 34, 55.  
and then stop at this last value and as soon as this last value is reached produce an output LED which is a logical 1.
- 2 Write a complete VHDL module for a variable divider. The divider is to be able to divide by any number between 64 and 127. The divider ratio is to be set by a 6- bit word, connected to input pins 25 to 30, with pin 30 being the most significant bit. The divider output is the most significant bit of the variable divider and is to be connected to pin 31. In addition a clock is connected to pin 11 and a reset to pin 35. The VHDL module should include the pin allocations.
- 3 An existing circuit produces a pulse of one clock-pulse width as shown in waveform A. The period of this waveform A, can be from 4 to 12 clock-pulses long. Design a circuit to:
  - 1 Count the number of clock-pulses in the period of the waveform A.
  - 2 Transfer this count to a series of 4 flip-flops to store the resulting count. (This is a latch)



Write the VHDL code to achieve this function.

- 4 It is desired to have two electronic dice, programmed as one VHDL design. The design should include the logic functions for all the required dots.



Stage 1: Design the VHDL code and produce the waveforms to demonstrate the operation.

Stage 2: Program the dice onto one of the EPLD boards used for labs. The lights A1, B1, C1, D1, E1, F1, G1 for the first die, should be connected to pins 3, 4, 5, 6, 7, 8, 9 on the EPLD board. The lights A2, B2, C2, D2, E2, F2, G2 for the second die, should be connected to pins 25, 26, 27, 28, 29, 30, 31.

On the EPLD board a clock is available at pin 11.

In addition pins 37 to 44 are connected to LED's on the EPLD board, and they can be used for testing features.

- 5 Design a 10 bit Pseudo Random Noise Generator using VHDL programming techniques. The 8 most significant bits of the PR generator are to be connected to the DAC on the development board. Fit this to the Lattice ispLSI2032 devices used on the EPLD board used in the labs and listen to the resulting output.

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